IPC/NETIPC-6A, -6L, -6H

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1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.
Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.
Syslogic is grateful for any help referring to errors or for suggestions for improvements.
The following registered trademarks are used:

IBM-PC, PC/AT, PS/2	trademarks of IBM Corporation
I^2C	trademark of Philips Corporation
CompactFlash	trademark of SanDisk Corporation
DiskOnChip	registered trademark of M-Systems LTD
PC/104	trademark of PC/104 Consortium
Geode	trademark of Advanced Micro Devices (AMD)
Windows CE	trademark of Microsoft Corporation
Windows XP Embedded	trademark of Microsoft Corporation

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the PC/104 system. It provides all information needed to configure, setup and program the IPC/NETIPC-6 processor board family. For complete information the documentation of the mounted communications and I/O boards must be consulted. In the following paragraphs all descriptions referenced to NETIPC apply to all the IPC/NETIPC-6 derivates.

1.3. Additional Products and Documents

1.3.1. Hardware Products

The following hardware products are useful together with the NETIPC processor board:
- NETIPC boot loader key (BOOTPLUG-1A, part of CUB/DOWNKIT-1A)
- NETIPC serial port cable (AT-Link cable, part of CUB/DOWNKIT-1A)
- PC/104 communication boards (contact Syslogic sales)
- PC/104 I/O boards (contact Syslogic sales)

1.3.2. Software Products

The following software products are useful together with the NETIPC processor board:
- IPC/NETIPCFW-6A: Firmware for NETIPC boards
- IPC/IOCOMSW-1A: Sample program code and utilities for x86 based PC/104 systems
- Operating Systems: check chapter 6.4 for a list of supported implementations.

1.4. Documents and References

1.4.1. Syslogic Documentation

The following documents are *required* for correct installation and operation of the NETIPC processor board:

- DOC/NETIPCFW6-E: User Documentation for NETIPC Firmware
- DOC/IPC_IOCOMSW-E: User Documentation for programming examples and utilities

1.4.2. Standards and Books

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
- IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org

- 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego), ISBN 0-929392-15-9
- 'PCI System Architecture' by Tom Shanley / Don Anderson (Mindshare, Inc.), ISBN 0-201-30974-2
-

1.4.3. Datasheets

- Audio Codec '97 Specification
  www.intel.com/design/chipsets/audio/
- Datasheet AMD Geode LX800 microprocessor
  http://www.amd.com/us-en/ConnectivitySolutions/ProductInformation/0,,50_2330_9863_13022%5E13073,00.html
- Datasheet AMD CS5536 companion chip
  http://www.amd.com/us-en/ConnectivitySolutions/ProductInformation/0,,50_2330_9863_13022%5E13054%5E13083,00.html
- Datasheet Intel 82551ER Fast Ethernet Controller
  http://www.intel.com/design/network/products/lan/docs/82551ER_docs.htm
- Datasheet Intel 82551IT Fast Ethernet Controller
  http://www.intel.com/design/network/products/lan/docs/82551it_docs.htm

1.5. Items delivered

- The NETIPC comes without cabling and enclosure. These additional items must be ordered separately and installed according to the respective user documentations. Or a fully operational and configured COMPACT system can be ordered (for example IPC/COMPACT6-1E). For further information please contact Syslogic sales.

1.6. Installation

The firmware configuration and download is described in the appropriate firmware documentation.

Important Note

Before applying power to the NETIPC system, all installed boards must be configured correctly and mounted (please consult corresponding User Documentations).

1.7. Safety Recommendations and Warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.
The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.
The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.
In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 8). Do not use or install the products if you are in doubt.
In any case of misuse of the products, the user is solely liable for the consequences.

1.8. Electro-Static Discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in a ESD protected environment. Otherwise a proper operation is not garanteed.

1.9. Life Cycle Information

1.9.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains an antistatic bag and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.9.2. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.

The main functionality of the IPC system is defined by the application programs running on the processor board. The application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.9.3. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (EMI and mechanical protection).

1.9.4. Warranty

Our products are covered by a world-wide manufacturers warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a serial number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

1.9.5. RoHS

The product of the IPC/NETIPC-6 family are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC).

1.9.6. Disposal and WEEE

At the end of the life span the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.
The products of the IPC/NETIPC-6 are not designed ready for operation for the end-user and intended for consumer applications. Therefore the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable. But users should still dispose the product properly at the end of life.

2 Product Description

2.1. NETIPC-6 Family Comparison

The NETIPC-6 boards are x86 based processor board designed for use with the IPC line of communications and I/O boards. Using the same form factor, it fits into all standard IPC enclosures to build up various industrial control system based on the standard PC/AT architecture.

The derivates differ in perfomance (mainly processor clock) and the amount of memory.

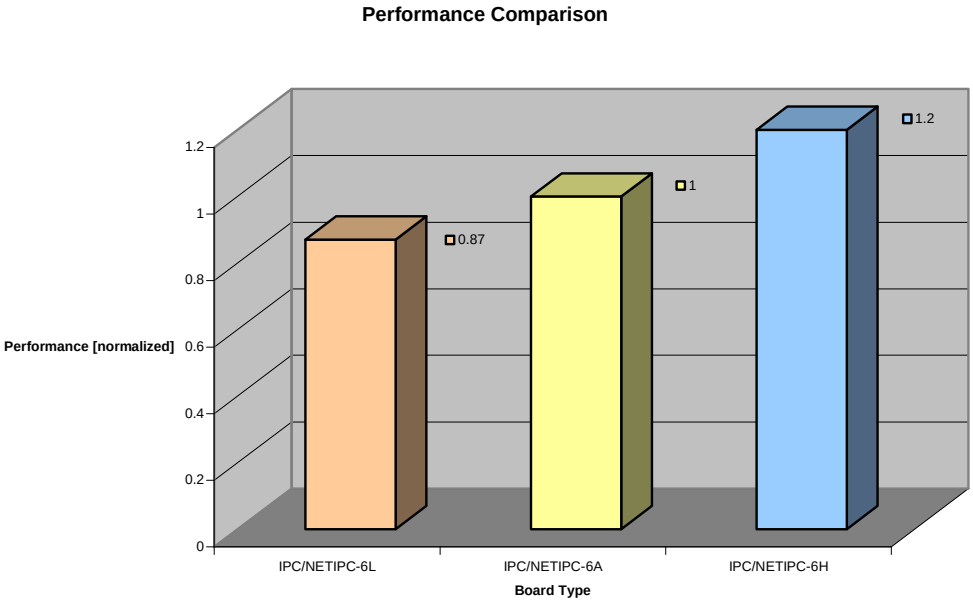

Fig. 1 Performance Comparison

A list of main features can be found below:

2.2. Features of the IPC/NETIPC-6L(N)

CPU Core

- AMD Geode LX700 @ 0.8W low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 8-stage pipeline x86 based processor core with efficient prefetch and branch prediction
- integrated Floating Point Unit (supports MMX and AMD 3Dnow! instruction sets
- 433MHz processor clock
- Split I/D L1 cache_64kB Instruction cache, 64kB Data cache
- Configurable L2 cache (I or D or both)
- 64-bit wide DDR SDRAM interface

Memory

- 128 Mbyte DRAM on board (DDR333, 167MHz)

Graphics Controller

- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

CompactFlash and IDE Interface

- Enhanced IDE interface (ATA-5 specification) supporting 2 IDE devices with PIO modes 0 to 4, MDMA modes 0 to 2 or UDMA modes 0 to 5
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support

Serial Ports
- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit fifo (16550)
- Two USB V2.0 ports (OHCI/EHCI-Host Controller)

Universal Serial Bus
Ethernet
- 10/100baseT Ethernet interface

Firmware Flash Memory
- 16 MBit BootBlock Flash for BIOS, BIOS extensions and 1.44 Mbyte ROM-drive A: (floppy replacement), supporting easy firmware update through serial port

Add-On Memory
- 32 pin DIL socket for user installable Socket Memory supporting various types of 32 and 28 pin SRAM and EEPROM devices from 32 kbyte up to 512 kbyte
- battery backed through Vbat pin on a PC/104 bus extension

Real Time Clock
- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through VBat pin on a PC/104 bus extension

PC/104 Interface
- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards

2.3. Features of the IPC/NETIPC-6A(N)

CPU Core
- AMD Geode LX800 @ 0.9W low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 8-stage pipeline x86 based processor core with efficient prefetch and branch prediction
- integrated Floating Point Unit (supports MMX and AMD 3Dnow! instruction sets
- 500MHz processor clock
- Split I/D L1 cache_64kB Instruction cache, 64kB Data cache
- Configurable L2 cache (I or D or both)
- 64-bit wide DDR SDRAM interface

Memory
- 256 Mbyte DRAM on board (DDR400, 200MHz)

Graphics Controller

- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

CompactFlash and IDE Interface
- Enhanced IDE interface (ATA-5 specification) supporting 2 IDE devices with PIO modes 0 to 4, MDMA modes 0 to 2 or UDMA modes 0 to 5
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

Integrated Peripherals
- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

PS/2 Mouse and Keyboard Interface
- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support

Serial Ports
- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit fifo (16550)
- Two USB V2.0 ports (OHCI/EHCI-Host Controller)

Universal Serial Bus
Ethernet
- 10/100baseT Ethernet interface

Audio Interface
- AC97 compatible sound port with Line In/Out, Speakers and Headphone pins

Firmware Flash Memory
- 16 MBit BootBlock Flash for BIOS, BIOS extensions and 1.44 Mbyte ROM-drive A: (floppy replacement), supporting easy firmware update through serial port

Add-On Memory
- 32 pin DIL socket for user installable Socket Memory supporting various types of 32 and 28 pin SRAM and EEPROM devices from 32 kbyte up to 512 kbyte
- battery backed through Vbat pin on a PC/104 bus extension

Real Time Clock

- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through VBat pin on a PC/104 bus extension

PC/104 Interface

- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards

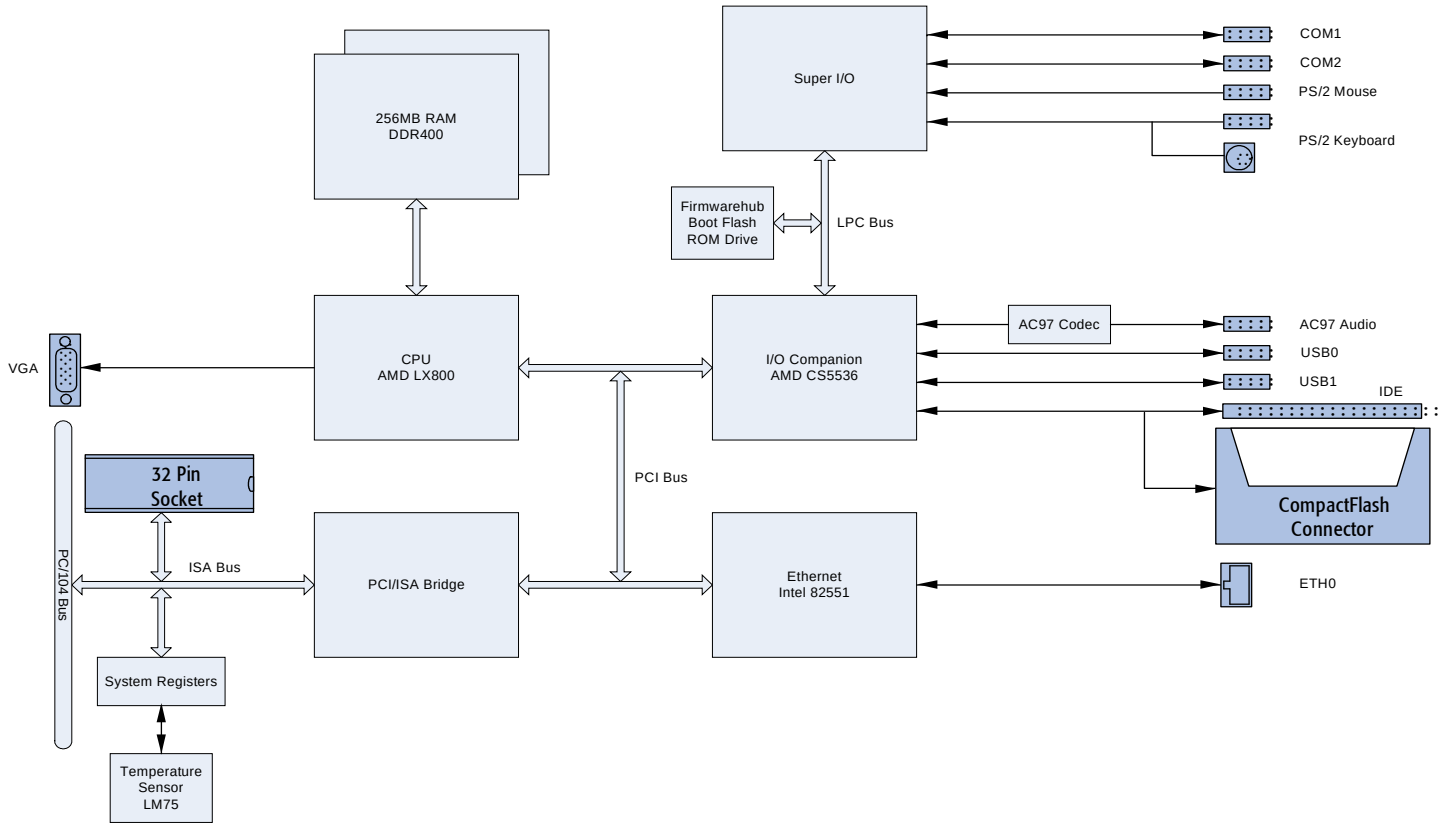

Fig. 2 Block Diagram (NETIPC-6A)

2.4. Features of the IPC/NETIPC-6H(N)

CPU Core

- AMD Geode LX900 @ 1.5W low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 8-stage pipeline x86 based processor core with efficient prefetch and branch prediction
- integrated Floating Point Unit (supports MMX and AMD 3Dnow! instruction sets
- 600MHz processor clock
- Split I/D L1 cache_64kB Instruction cache, 64kB Data cache
- Configurable L2 cache (I or D or both)
- 64-bit wide DDR SDRAM interface

Memory

- 512 Mbyte DRAM on board (DDR400, 200MHz)

Graphics Controller

- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1920x1440x32 bpp at 85Hz and 1600x1200x32 bpp at 100Hz

CompactFlash and IDE Interface

- Enhanced IDE interface (ATA-5 specification) supporting 2 IDE devices with PIO modes 0 to 4, MDMA modes 0 to 2 or UDMA modes 0 to 5
- standard 44 pin IDE (2mm) connector for two external IDE devices
- CompactFlash Type I connector for onboard mountable CompactFlash card configurable as master or slave IDE device (replacing one of the external IDE devices)

Integrated Peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

PS/2 Mouse and Keyboard Interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support

Serial Ports

- Two serial RS232 ports (COM1, COM2) with 16 byte receive and transmit fifo (16550)

- Two USB V2.0 ports (OHCI/EHCI-Host Controller)

Universal Serial Bus
Ethernet
- 10/100baseT Ethernet interface

Audio Interface
- AC97 compatible sound port with Line In/Out, Speakers and Headphone pins

Firmware Flash Memory
- 16 MBit BootBlock Flash for BIOS, BIOS extensions and 1.44 Mbyte ROM-drive A: (floppy replacement), supporting easy firmware update through serial port

Add-On Memory
- 32 pin DIL socket for user installable Socket Memory supporting various types of 32 and 28 pin SRAM and EEPROM devices from 32 kbyte up to 512 kbyte
- battery backed through Vbat pin on a PC/104 bus extension

Real Time Clock
- Year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through VBat pin on a PC/104 bus extension

PC/104 Interface
- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards

2.5. Operating Modes

The NETIPC is based on the standard PC/AT architecture and therefore operates in DOS-compatible mode (real mode) on start up. The configurable BIOS initializes all onboard peripherals to their default values, executes the BIOS extensions programmed into the onboard Boot Block Flash by the user and BIOS extensions found on installed expansion boards prior to booting the operating system from a user-selectable drive (boot sector or OS image file). The operating system (or eventually a BIOS extension) may switch to protected mode to execute high performance 32-bit program code.

2.6. Startup Modes

The NETIPC-6 doesn't support any special startup modes.

3 Hardware Description

3.1. Overview

The NETIPC board hardware may be configured by software (BIOS) and by jumper setting. Software configuration should always be done using the BIOS configuration program freely available as part of the NETIPC firmware package IPC/NETIPCFW-6A, unless the BIOS does not support it (see firmware documentation DOC/NETIPCFW6 for details about supported BIOS configuration options).
The jumper and connector locations are shown in the board layout drawing (Fig. 3).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

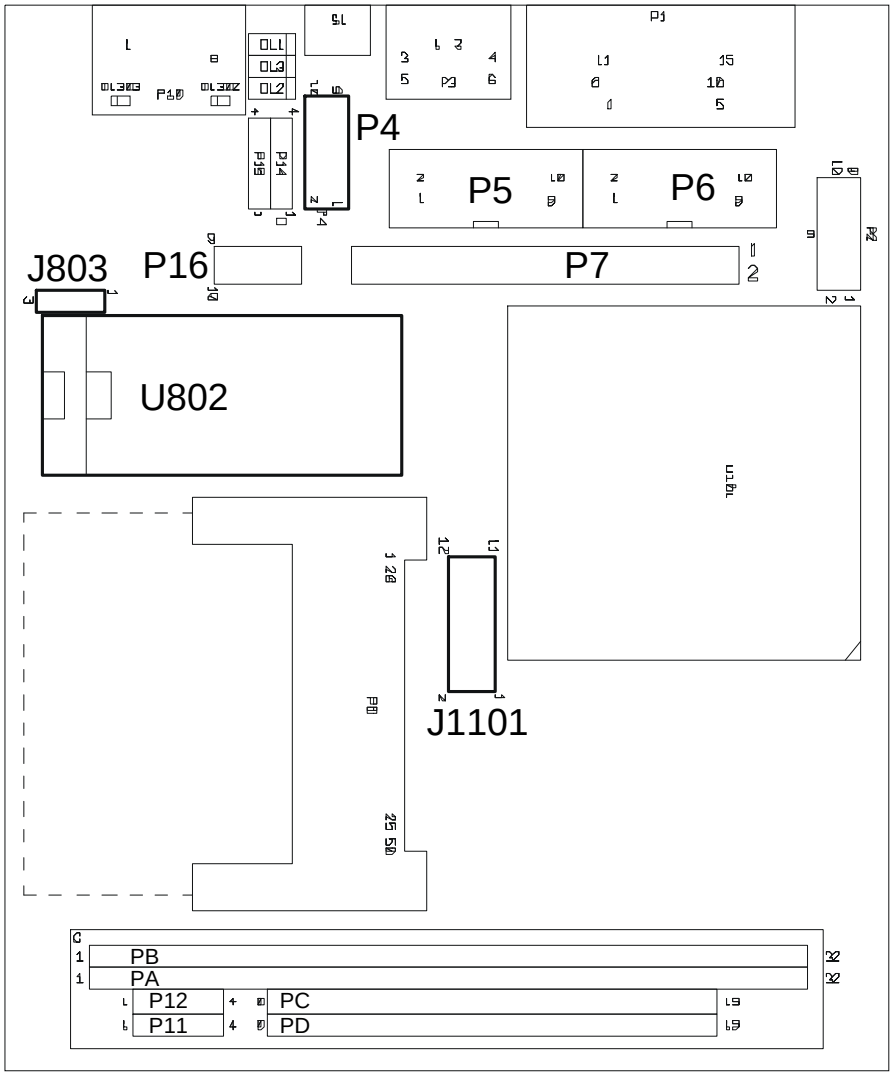

Fig. 3 Board Layout (NETIPC-6A)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The NETIPC uses the same memory layout as a standard desktop PC. Four onboard devices , DRAM, graphics controller, Boot Block Flash and Socket Memory, make use of the 4 GByte adressable memory space.

Address	Device / Register	Remarks
0000'0000..0009'FFFFh	640 kByte Main Memory (DRAM)	
000A'0000..000B'FFFFh	Video Memory	
000C'0000..000D'BFFFh	Configurable memory range (BIOS, BIOS Extensions, DRAM, Socket Memory or redirected to PC/104 bus)	see paragraph 3.7.1 and 4.2.3
000D'C000..000F'FFFFh	BIOS	do not write
0800'0000..807F'FFFFh	Reserved	do not access
8080'0000..8087'FFFFh	Socket Memory	
8088'0000..83EF'FFFFh	Reserved	do not access
FFE0'0000..FFF7'FFFFh	1.44 Mbyte Firmware Flash	ROM drive
FFF8'0000..FFFF'FFFFh	BIOS/BIOS Extensions	do not access

Tab. 1 Physical Memory Address Space Layout

Address	Device / Register	Remarks
0010'0000…06BF'FFFFh	107 MByte Main Memory (DRAM)	IPC/NETIPC-6L(N): free Memory above 1M
06C0'0000..07BF'FFFFh	16MB Graphic Memory	do not access
07C0'0000..07FF'FFFFh	4MB SMM, Firmbase, VSA	do not access

Tab. 2 IPC/NETIPC-6L(N) Specific Physical Memory Address Space Layout

Address	Device / Register	Remarks
0010'0000..0EBF'FFFFh	235 MByte Main Memory (DRAM)	IPC/NETIPC-6A(N): free Memory above 1M
0EC0'000..0FBF'FFFFh	16MB Graphic Memory	do not access
0FC0'0000..0FFF'FFFFh	4MB SMM, Firmbase, VSA	do not access

Tab. 3 IPC/NETIPC-6A(N) Specific Physical Memory Address Space Layout

Address	Device / Register	Remarks
0010'0000…01EAF'FFFFh	491 Mbyte Main Memory (DRAM)	IPC/NETIPC-6H(N): free Memory above 1M
01EB0'000..01FAF'FFFFh	16MB Graphic Memory	do not access
01FB0'0000..01FFF'FFFFh	4MB SMM, Firmbase, VSA	do not access

Tab. 4 IPC/NETIPC-6H(N) Specific Physical Memory Address Space Layout

Important Note

The main memory above 1M isn't fully usable for applications. The main memory for applications is shared with the graphics memory (UMA: Unified Memory Architecture). The graphics memory can be configured from 4MB to 60MB. The default value is 16MB.
Firmbase and System Management Mode software and drivers for Geode's VSA (Virtual System Architecture) are located at the top of the extended memory range (e.g. 4MB). The graphic memory Size can configured in the BIOS. To calculate the remaining memory space the graphic memory size and 4MB of the Firmbase/SMM/VSA must be subtracted from the memory top.
IPC/NETIPC-6A example: With the graphics memory size of 16 MByte (default), usable main memory ends at address:
- 0EBF'FFFFh (235 Mbyte free main memory)
This must be considered in operating system configuration (e.g. Windows CE).
Depending on Shadowing configuration the effective size may be slightly higher.

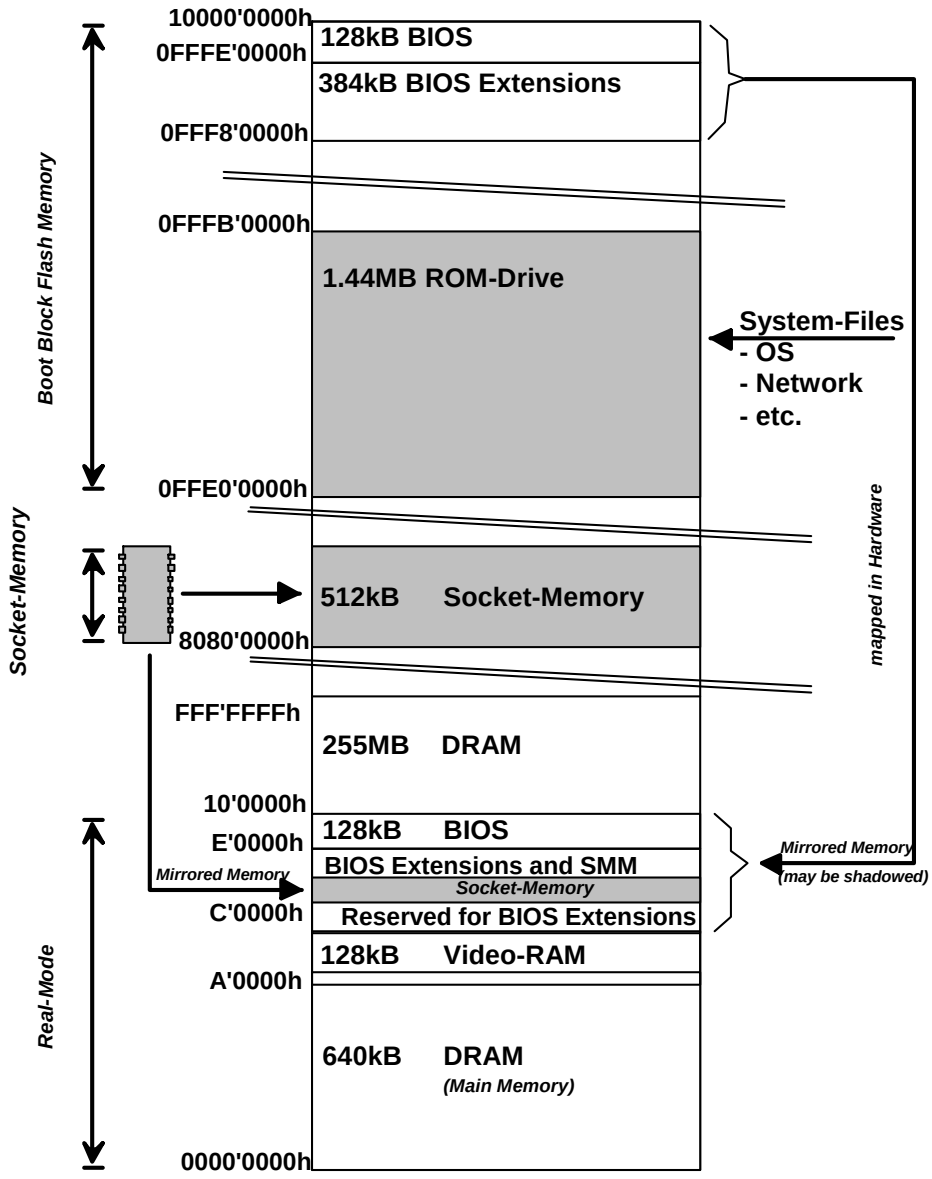

Fig. 4 Memory Map (IPC/NETIPC-6A board)

3.2.2. General I/O Layout and Configuration

The NETIPC's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Device / Register	Remarks
0000..000Fh	Slave DMA	
0020h	PIC Master – Command/Status	
0021h	PIC Master – Command/Status	
0040..0043h	PIT	
0060h	Keyboard/Mouse – Data Port	
0061h	Port B Control	
0064h	Keyboard/Mouse – Command/Status	
0070.0.071h	RTC RAM Addres/Data Port	
0072..0073h	High RTC RAM Address/Data Port	
0080h	Post Code Display	
0081..0083h	DMA Low Page	
0087h	DMALow Page	
0089..008Bh	DMA Low Page	
008Fh	DMA Low Page	
0092h	Port A	
00A0h	PIC Slave – Command/Status	
00A1h	PIC Slave – Command/Status	
00C0h	Master DMA	
00C2h	Master DMA	
00C4/00C6h	Master DMA	
00C8/00CA	Master DMA	
00CCh	Master DMA	
00CEh	Master DMA	
00D0h	Master DMA	
00D2h	Master DMA	
00D4h	Master DMA	
00D6h	Master DMA	
00D8h	Master DMA	
00DAh	Master DMA	
00DCh	Master DMA	
00DEh	Master DMA	
0200..023Fh	free	avail. on PC/104 bus
0278..027Fh	Reserved for LPT2	not available
02E0..02E7h	free	avail. on PC/104 bus
02E8..02Efh	Reserved for COM4	avail. on PC/104 bus
02F8..02FFh	COM2	
0370..0372h	Reserved for Floppy 2	
374..375h	Reserved for Floppy 2	
0377h	Reserved for Floppy 2	

0378..037Fh	Reserved for LPT1	avail. on PC/104 bus
03B0..03BBh	VGA Registers (MDA)	
03BC..03BFh	Reserved for LPT3	
03C0..03CFh	VGA registers (EGA)	
03D0..03DFh	VGA registers (CGA)	
03E0..03E7h	free	avail. on PC/104 bus
3E8..03EFh	Reserved for COM3	avail. on PC/104 bus
03F0.0.3F2h	Reserved for Floppy 1	
03F4..03F5h	Reserved for Floppy 1	
03F6h..03F7h	Primary IDE Channel	
03F7h	Reserved for Floppy 1	
03F8..03FFh	COM1	
0481..0483h	DMA High Page	
0487h	DMA High Page	
0489..048Bh	DMA High Page	
048Fh	DMA High Page	
04D0h 04D1h	PIC Level/Edge PIC Level Edge	
0500..07FF	Runtime Registers Super I/O	
0A78h	Plug'n Play configuration port	
0CF8..0CFFh	PCI configuration registers	
7600..767Fh	not used	avail. on PC/104 bus
8200..827Fh	NETIPC system registers	avail. on PC/104 bus
0D000..0EFFFh	reserved for PCI devices (VGA, Ethernet, USB, IDE)	

Tab. 5 I/O Address Space Layout

Only the I/O addresses which are marked with “avail. On PC/104 bus” can be accessed on the aforementioned connector and be used for additional peripherals. The other unused I/O space can’t be access because these cycles are claimed by the integrated South Bridge and not by the PCI/ISA Bridge.

3.3. AMD Geode LX800 CPU

The AMD Geode LX processors are highly integrated x86 processors for embedded applications. The LX800 integrates the core microprocessor and the north bridge into one device.

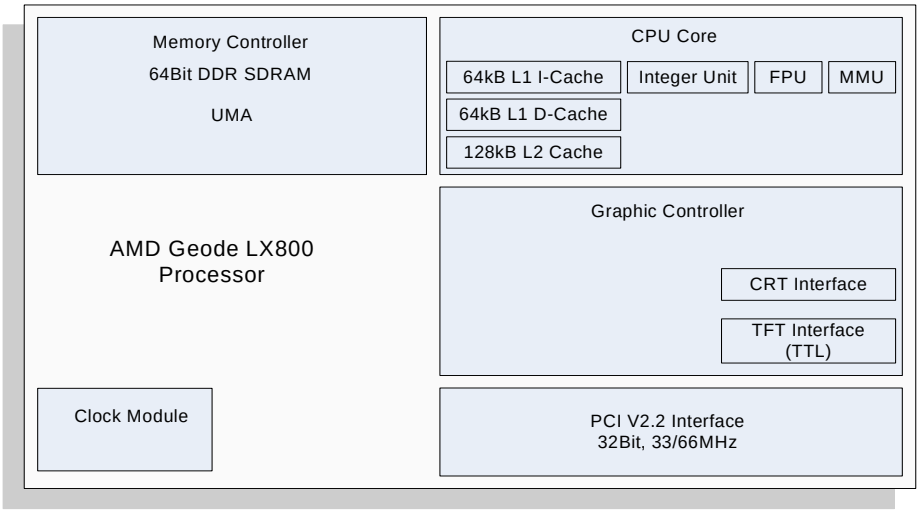

Fig. 5 AMD Geode LX800 processor

3.4. AMD CS5536 Companion Chip

The AMD Geode CS5536 companion device is designed to work with the LX800 microprocessor.

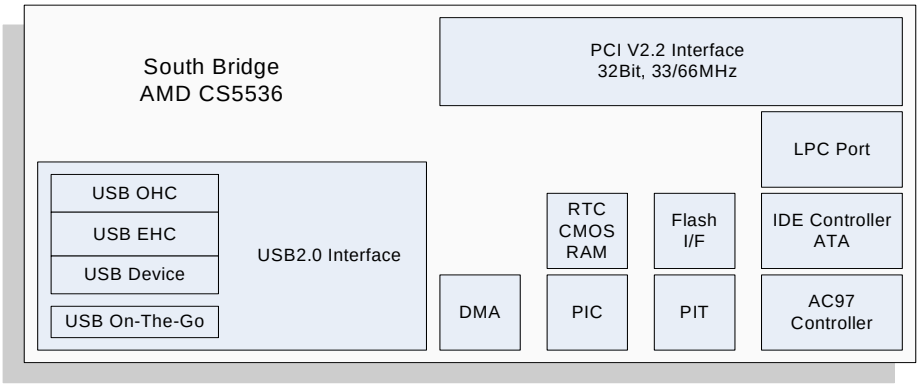

Fig. 6 AMD Geode CS5536 companion chip

3.5. PCI Devices

All devices follow the PCI 2.2 specification. The BIOS (and/or OS) control memory and I/O resources.

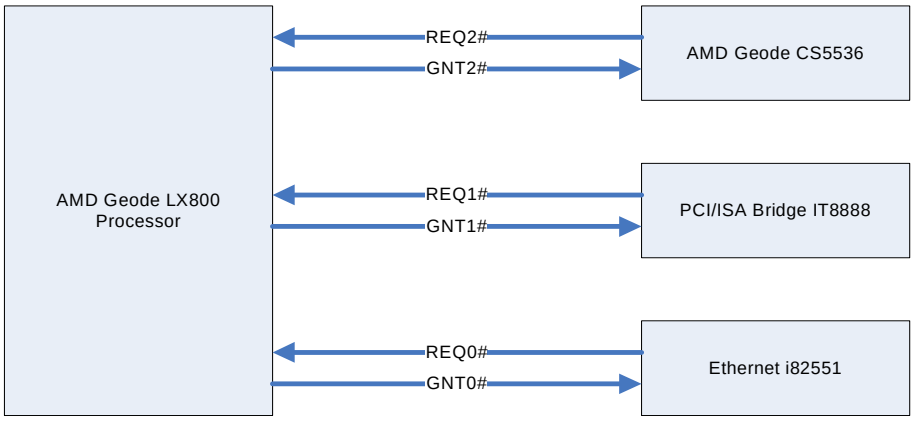

Fig. 7 PCI System

PCI Device (IDSEL)	Device ID	PCI IRQ	REQ / GNT	Comment
Host Bridge	2080h	n/a	2	Integrated in chipset
Graphic Controller	2081h	INTA# (IRQ9)	n/a	Integrated in chipset
Encryption Controller	2082h	INTA# (IRQ9)	n/a	Integrated in chipset
Ethernet Controller (AD23)	1209h	INTB# (IRQ10)	0	Intel 82551
PCI/ISA bridge (AD24)	0628h	n/a	1	IT8888
PCI/ISA bridge	2090h	n/a	n/a	Integrated in chipset
IDE Controller	209Ah	n/a	n/a	Integrated in chipset
Audio Controller	2093h	INTA# (IRQ9)	n/a	Integrated in chipset
USB Controller	2094h	INTD# (IRQ7)	n/a	Integrated in chipset
USB Controller	2095h	INTD# (IRQ7)	n/a	Integrated in chipset

Tab. 6 PCI Devices

3.6. Hardware Interrupts

The AMD Geode LX800 chipset integrates two legacy 8259-compatible Programmable Interrupt Controllers (PIC). The registers of the PIC can be accessed through the I/O ports 020h and 021h resp. 0A0h and 0A1h.

Device	IRQ	PCI IRQ	Comment
8254 Timer	0	-	Legacy
Keyboard	1	-	Legacy
8259	2	-	Slave controller
UART	3	-	COM2
UART	4	-	COM1
Free	5	-	Available on PC/104 bus
Free	6	-	Available on PC/104 bus
USB	7	PCI INTD#	Do not used for with devices
RTC	8	-	Legacy
Grahip Controller	9	PCI INTA#	Shared with Encryption and Audio Controller
Ethernet	10	PCI INTB#	Do not use with other devices
Free	11	-	Available on PC/104 bus
Mouse	12	-	Legacy
FPU	13	-	Legacy
IDE	14	-	Primary IDE channel
Free	15	-	Available on PC/104 bus

Tab. 7 Hardware Interrupt Table

3.7. Peripheral Devices

3.7.1. Socket Memory

The NETIPC features a DIL32 socket (U802) for user insertable memory devices like SRAM, NVRAM and EEPROM products. Supported devices and corresponding configuration is listed in the table below, maximum access time allowed is 150 ns for all devices. Note that the Socket Memory base address, size and enabling must also be configured by software (BIOS).

Memory Type	Manufacturer and Order Code	J1101 Setting (pins 8, 9,10,12 only)	J803 Setting
SRAM	**Static RAM (5V)**	**5V, Battery Backup enabled**	
128k x 8	Samsung: K6X1008C2D-DB70 Hitachi: HM628128BLP-7 STMicro: M68AF127BL70B6	8-10	2-3
512k x 8	Samsung: K6T4008C1C-DB70 Hitachi: HM628512BLP-7 Mitsubishi: M5M5408AP-70L	8-10	1-2
NVRAM	**Nonvolatile RAM (5V)**	**5V, Battery Backup disabled**	
32k x 8	ZMD: U637256DC70	9-10	2-3
32k x 8	Simtek: STK16C88-W45	9-10	2-3
NVRAM	**Nonvolatile RAM (3.3V)**	**3.3V, Battery Backup disabled**	
128k x 8	Simtek: STK16CA8-W45	10-12	2-3
EEPROM	**EEPROM (5V)**	**5V, Battery Backup disabled**	
32k x 8	Atmel: AT28C256(E)-15PC Catalyst: CAT28C256(H)P-15 Hitachi: HN58C256AP-10 ST: M28256-15BS Xicor: X28C256P-15	9-10	2-3
64k x 8	Catalyst: CAT28C512(H)P-15 SST: SST29EE512A-90-4C-PH Xicor: X28C512P-15	9-10	2-3
128k x 8	Atmel: AT28C010(E)-15PC SST: SST29EE010A-120-4C-PH Xicor: X28C010D-15	9-10	2-3

Tab. 8 Socket Memory Configuration

Important Note

Do not insert devices not listed. This could damage the hardware.

Important Note

For DiskOnChip device support plese contact the manufacturer.

Important Note

When inserting a 28 pin device into the 32 pin socket, pin 1 of the 28 pin device must be positioned at pin 3 of the DIL32 socket, otherwise the hardware may get damaged.

3.7.2. VGA Interface

The VGA signals are available on the High Density DSUB15 connector P1 for direct connection of VGA compatible monitors. The signals are also available on the internal header P2 for special expansion boards that may convert the VGA signals into other display standards (e.g. PAL/NTSC or digital TFT). The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).

Device Connection

Pin Number	Signal	Remarks
1	RED	
2	GREEN	
3	BLUE	
4	-	
5	GND	
6	GND	
7	GND	
8	GND	
9	+5V	not fused
10	GND	
11	-	
12	DDC Data	
13	HSYNC	
14	VSYNC	
15	DDC Clock	

Tab. 9 VGA connector P1 (DSUB15HD)

Pin Number	Signal	Pin Number	Signal
1	RED	2	GREEN
3	BLUE	4	GND
5	Not used	6	GND
7	HSYNC	8	VSYNC
9	DDC Data	10	DDC Clock

Tab. 10 VGA internal Header P2 (2x5 pin)

Important Note

Check the P2 header type (2x5 pin) and signals in table Tab. 10 before connecting anything.

Important Note

Be careful when using the VGA or video signals on expansion boards. Special design and layout precautions must be met for these high speed analog signals.
Maximum cable length allowed for VGA connection is 15 m.
Use high quality VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

3.7.3. IDE/CompactFlash-Interface

The IDE interface is setup as Primary IDE Channel with standard PC address decoding and using hardware interrupt 14. It supports 2 external devices on a single connection, one configured as master the other as slave. Alternatively one external device may be replaced by an on board pluggable CompactFlash card. The IDE timing is setup by software (BIOS autodetection).
The IDE interface provides the following configuration options:

Configuration Options

Jumper	Configuration	Remarks
J1101	Pin 2-4 open = on board CompactFlash is slave Pin 2-4 closed = on board CompactFlash is master	don't care if only external devices are connected.

Tab. 11 IDE Configuration Options

Device Connection

External IDE devices are connected through the standard 2x20 pin header J15. A CompactFlash card may be directly plugged in the on board CompactFlash connector P8.

Pin Number	Signal	Pin Number	Signal
1	RST#	2	GND
3	HD7	4	HD8
5	HD6	6	HD9
7	HD5	8	HD10
9	HD4	10	HD11
11	HD3	12	HD12
13	HD2	14	HD13
15	HD1	16	HD14
17	HD0	18	HD15
19	GND	20	NC
21	DRQ	22	GND
23	HIOW#	24	GND
25	HIOR#	26	GND
27	IOCHRDY	28	GND
29	DACK#	30	GND
31	IRQ	32	NC
33	HA1	34	PDIAG#
35	HA0	36	HA2
37	HCS0#	38	HCS1#
39	DASP#	40	GND
41	VCC	42	VCC
43	GND	44	NC

Tab. 12 IDE Connector P7 (2x22 pin)

Important Notes

Do not connect 2 external devices and a CompactFlash card together. This may damage the system and the IDE devices.

Note

The NETIPC offers a 5V supply (not fused) for direct plugin IDE/CompactFlash adapters. Max. allowed current drawing is 100mA.

3.7.4. Serial Ports

Two serial ports are available. The serial ports have fixed base addresses of 3F8H for COM1 and 2F8H for COM2. COM1 uses hardware interrupt 4 and COM2 uses hardware interrupt 3.

Device Connection

The Serial Port COM1 is available on the internal header P5.
The Serial Port COM2 is available on the internal header P6.

Pin Number	Signal	Pin Number	Signal
1	DCD*	2	DSR*
3	RXD	4	RTS*
5	TXD	6	CTS*
7	DTR*	8	RI*
9	GND	10	+5V (not fused)

Tab. 13 Serial Port COM1 and COM2 internal Headers P5, P6 (2x5 pin)

3.7.5. Keyboard/Mouse Interface

The keyboard signals are available on the MiniDIN connector P3 for direct connection of PS/2 style keyboards. The PS/2-mouse signals are available on the internal header P4. The controller uses hardware interrupt 1 for the keyboard and hardware interrupt 12 for the mouse. The following configuration options are provided:

Configuration Options

Jumper	Configuration	Remarks
P4	Pin 1-3, 2-4 closed = Keyboard signals on P3 Pin 3-5, 4-6 closed = Mouse signals on P3	

Tab. 14 Keyboard/Mouse Configuration Options

Device Connection

The standard PS/2 connector P3 is used for direct connection of the keyboard or mouse (depending on jumper configuration). The Keyboard/Mouse signals are also available on the internal 2x5 pin header P4 for connection of the other device. P3 is not available on NETIPC-6AD, use P4 instead.

Pin Number	Signal	Remarks
1	KBDATA / MDATA	
2	- (Boot Mode Pin BM1)	do not connect
3	GND	
4	+5V (not fused)	
5	KBCLK / MCLK	
6	- (Boot Mode Pin BM0)	do not connect

Tab. 15 Keyboard/Mouse connector P3 (PS/2)

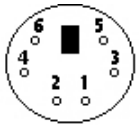

Fig. 8 6-pin female Mini-DIN (PS/2) socket (front view)

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	BM1 / P3-2	8	BM0 / P3-6
9	GND	10	+5V (not fused)

Tab. 16 Keyboard/Mouse internal Header P4 (2x5 pin)

Important Note

Do not connect the Boot Mode Pins on P3 or P4. These signals may only be used by the Boot Loader Key to start the Boot Loader.
The Boot Loader Key (BOOTPLUG) shortens Pin 3 and 6 of P3.

Important Note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
Use shielded cables for maximum EMI protection.

3.7.6. USB Interface

The NETIPC-6A features an OHCI/EHCI compatible USB Hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS.

Device Connection

The USB interface uses two 4pin headers for the two USB channels.

P14	USB channel 0	P15	USB channel 1
Pin Number	Signal	Pin Number	Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 17 USB Interface Connector P14/P15 (1x4pin/1x4pin)

3.7.7. Ethernet Interface

The NETIPC-6A features a PCI Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. The Ethernet interface also features a yellow LED on the front panel to indicate Good Link (on) and Line Activity (flashing). There are two additional LED's (yellow and green) integrated into the RJ45 connector. With these two boards, the meaning of the LED activity is programmable (normally set by the low level driver).
No configuration options are available for the ethernet device.

Device Connection

The Ethernet interface uses the standard RJ45 connector P10 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 18 Ethernet Twisted Pair Interface Connector P10 (RJ45)

3.7.8. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the NETIPC's hardware reset or the processors NMI line depending on software configuration.

Configuration Options

Jumper	Configuration	Remarks
J1101	Pin 4-6 open = 1.6 s Pin 4-6 closed = 100 ms	

Tab. 19 Watchdog Configuration Options

3.7.9. Sound Port

The Sound Port uses a AC97 v2.1 compatible Codec which supports 18bit data streams at a sampling rate of 48kHz.
No hardware configuration options are available for the Sound Port.

Device Connection

The Sound Port uses a 2x5pin header.

P16 Pin Number	Signal	P16 Pin Number	Signal
1	VCCA	2	AGND
3	MIC_IN	4	MIC_BIAS
5	HP_OUT_R	6	HP_OUT_L
7	LINE_IN_R	8	LINE_IN_L
9	LINE_OUT_R	10	LINE_OUT_L

Tab. 20 Sound Port Connector P16 (2x5pin)

3.7.10. PC/104 Bus Interface

The PC/104 bus interface of the NETIPC allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in Tab. 21. For single board applications only the power pins should be connected. See paragraph 5.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
P11			P12			A2	⊗	SD7	B2	⊗	RESETDRV
1	⊗	GND	1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
2	⊗	no connection	2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
3	⊗	no connection	3	⊗	TRIGGER*	A5	⊗	SD4	B5	⊗	-5V (not used)
4	⊗	Vbatt	4	⊗	STOP*	A6	⊗	SD3	B6	⊗	DRQ2
						A7	⊗	SD2	B7	⊗	-12V (not used)
						A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (not used)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
						A29	⊗	SA2	B29	⊗	+5V
						A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 21 PC/104 Bus Connectors PA/PB, PC/PD

Important Note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the NETIPC board or add-on boards.

The battery backup supply for the onboard Real Time Clock and SRAM must be connected to connector P11 as follows (also see Tab. 21) :

Pin Number	Signal	Remarks
1	GND	
2	no connection	
3	no connection (KEY)	
4	Vbatt	

Tab. 22 External Battery Connector P11 (1x4 pin)

The user programmable output signals STOP* and TRIGGER* are available on connector P12. The signal levels are TTL compatible with maximum 4 mA sink and 2 mA source output current (also see Tab. 21) :

Pin Number	Signal	Remarks
1	GND	
2	+5V	max. 10 mA
3	TRIGGER*	
4	STOP*	

Tab. 23 User Programmable Output Connector P12 (1x4 pin)

The TRIGGER* signal may be controlled by software or by a hardware timer, e.g. Timer Channel 2 Out (Speaker Drive) or Real Time Clock SQW output (see chapter 4).
A speaker may be connected to this signal if buffered with an external NPN transistor or inverting power driver.

3.7.11. Factory Programming Header

The programmable logic devices on the NETIPC board are factory programmed using some pins of the internal header J1101. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK	do not use
3	TDO	do not use
5	TMS	do not use
7	TDI	do not use

Tab. 24 Factory Programming Header J1 (2x5 pin)

3.8. Hardware Limitations

3.8.1. PCI Bus Limitations

- Only 3.3V PCI bus
- PCI bus speed is limited to 33MHz
- No PCI bus connector is provided

3.8.2. ISA Bus (PC/104) Limitations

The NETIPC board is not fully IEEE 996.1 (PC/104) compliant. The following restrictions and differences to the IEEE 996.1 specification apply:

- connector and mounting holes are compatible but the board dimensions are bigger (100 x 120 mm^2)
- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)
- NMI (IOCHCK#) is not supported on the PC/104
- Only a predefined amount of I/O addresses are available on the PC/104 bus, please refer to the appropriate chapter for details

4 Programming Information

4.1. Overview

The programming of the NETIPC board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS. For detailled information refer to the NETIPC firmware documentation and other related documents as listed in paragraph 1.3.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

Please refer to chapter 3.6 for the table showing the usage of the NETIPC's interrupts.

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming Geode internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the NETIPC system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 4.3. Note that the Socket Memory related registers are programmed by the BIOS on system startup and must not be changed during operation except for the Socket Memory Window Mapping Register in case of user controlled memory mapping (allowing access to 512kbyte Socket Memory as eight 64kbyte blocks in the Socket Memory window below 1M in Real Mode).

Address	Device / Register	Remarks
8200h	Status Register	
8201h	Control Register	Reset state = 05H
8202h	Function ID Register	
8203h	reserved	do not write
8204h	Option ID Register	
8205h	Setup Register	Reset state = 00H
8206h	Revision ID Register	
8207h	Socket Memory Configuration Register	Reset state = 00H
8208h	Socket Memory Window Mapping Register	Reset state = 00H
8209h	Socket Memory Window Base Address Register	Reset state = D0H
820Ah	Boot Mode Input Register	
820Bh	I2C Register	for Temp Sensor
820C..821Fh	reserved	do not access

Tab. 25 NETIPC System Registers

Status Register

Reading I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
OVERTMP*	LOBAT*	1	WDG*	ERRFLAG*	ATTFLAG*	ERRINT*	ATTINT*

Description:

- ATTINT*: Attention Interrupt Status
  not used, returns 1
- ERRINT*: Error Interrupt Status
  0 = Error Interrupt pending on this module
  1 = no Error Interrupt pending on this module
- ATTFLAG*: Attention Status Flag (for polled applications)
  not used, returns 1
- ERRFLAG*: Error Status Flag (for polled applications)
  not used, returns 1
- WDG*: Watchdog Status Flag
  0 = Watchdog has timed out
  1 = Watchdog running or disabled
  Reset by issuing a hardware reset (see register 8204H)
- LOBAT*: Battery Status Flag
  0 = Battery voltage low
  1 = Battery voltage ok
- OVERTMP*: Temperatur Sensor Status Flag
  0 = programmed temperatur limit reached
  1 = temperatur ok (below limit)

Writing I/O Register 8200h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Control Register

Reading I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP	*TRIGSRC*	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used, returns 1
- ERREN*: Error Interrupt Enable (IOCHCK* routed to NMI)
  0 = Error interrupt on NMI enabled (always enabled)
- FREEZE: not used, returns 1
- *TRIGSRC: NETIPC TRIGGER* Signal Source Select*
  always 1
- STOP: NETIPC STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  0 = Watchdog timeout activates hardware reset
  1 = not supported
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)
- *TRIGGER: Direct Control for NETIPC TRIGGER* Signal*
  always 1

Writing I/O Register 8201h:

D7	D6	D5	D4	D3	D2	D1	D0
TRIGGER	WDTRIG	WDNMI	STOP	*TRIGSRC*	FREEZE	ERREN*	ATTEN*

Description:

- ATTEN*: Attention Interrupt Enable
  not used
- ERREN*: Error Interrupt Enable (IOCHCK* routing to NMI)
  0 = enable Error interrupt on NMI (always enabled)
- FREEZE: not used
- *TRIGSRC: NETIPC TRIGGER* Signal Source Select*
  always write 1
- STOP: NETIPC STOP* Signal State
  0 = STOP* inactive (high)
  1 = STOP* active (low)
- WDNMI: Watchdog action Select
  always write 0
- WDTRIG: Watchdog Trigger
  any state change triggers the watchdog (timeout reset)

- TRIGGER: Direct Control for NETIPC TRIGGER* Signal
  (if enabled by TRIGSRC bit in Control Register)
  always write 1

The Trigger feature is not supported on the IPC/NETIPC-6 boards.

TRIGSRC	***TRIGGER***	***TRIGGER* Source***
0	*0*	*Square Wave Output (SQW) of Real Time Clock Device*
0	*1*	*Timer (8254) Channel 2 Output gated with Port B bit 1 (Speaker Enable)*
1	*X*	*TRIGGER bit directly controls the TRIGGER* output*

Tab. 26 TRIGGER* Source Selection

Function ID Register

Reading I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
FID7	FID6	FID5	FID4	FID3	FID2	FID1	FID0

Description:

- FID7..0: Function ID
  0101'0001 (51h) = general NETIPC board,
  subtype defined by Option ID Register

Writing I/O Register 8202h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Option ID Register

Reading I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
OPT7	OPT6	OPT5	OPT4	OPT3	OPT2	OPT1	OPT0

Description:

- OPT7..0: Option ID
  1010'1000 (A8h) = IPC/NETIPC-6L, 128MB (if FID = 51h)
  1010'1001 (A9h) = IPC/NETIPC-6A, 256MB (if FID = 51h)
  1010'1010 (AAh) = IPC/NETIPC-6H, 512MB (if FID = 51h) (reserved)

Writing I/O Register 8204h:

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X

Description:

- xxxxxxxx: Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

Setup Register

Reading I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	0	0	0	0	0	0

Description:

- WDEN: Watchdog Enable
  0 = Watchdog disabled
  1 = Watchdog enabled (running)
- READY: NETIPC READY Signal State
  0 = READY inactive
  1 = READY active

Writing I/O Register 8205h:

D7	D6	D5	D4	D3	D2	D1	D0
READY	WDEN	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0
- WDEN: Watchdog Enable
  0 = Watchdog disabled (cannot be disabled while running)
  1 = enable Watchdog
- READY: NETIPC READY Signal State
  0 = deactivate READY
  1 = activate READY

Revision ID Register

Reading I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
RID7	RID6	RID5	RID4	RID3	RID2	RID1	RID0

Description:

- RID7..0: Revision ID
  xxH = Logic Design revision ID (see Tab. 32)

Writing I/O Register 8206h:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, always write 0

Socket Memory Configuration Register

Reading I/O Register 8207h:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = Window disabled below 1 M
  1 = Window enabled below 1 M

Writing I/O Register 8207h:

D7	D6	D5	D4	D3	D2	D1	D0
SOCKEN	0	0	0	0	0	0	MSIZE

Description:

- MSIZE: Socket Memory Window Size (below 1 M)
  0 = 32 kbyte
  1 = 64 kbyte
- SOCKEN: Socket Memory Window Enable
  0 = disable Window below 1 M
  1 = enable Window below 1 M

Socket Memory Window Mapping Register

Reading I/O Register 8208h:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Writing I/O Register 8208h:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	MMR2	MMR1	MMR0

Description:

- MMR2..0: Socket Memory Window Mapping Bit 2..0
  enables mapping of eight 64 kbyte pages (= 512 kbyte)

Socket Memory Window Base Address Register

Reading I/O Register 8209h:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..DBFFFh

Writing I/O Register 8209h:

D7	D6	D5	D4	D3	D2	D1	D0
1	1	MBAS5	MBAS4	MBAS3	MBAS2	MBAS1	MBAS0

Description:

- MBAS7..0: Socket Memory Window Base Address Bit 19..12
  range C0000..DBFFFh

Boot Mode Input Register

Reading I/O Register 820Ah:

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	BM1	BM0

Description:

- BM1..0: Boot Mode Inputs
  0 = reserved (Factory Diagnostic Mode)
  1 = reserved
  2 = Boot Loader Mode
  3 = normal Operating Mode

Writing I/O Register 820Ah:

D7	D6	D5	D4	D3	D2	D1	D0
reserved	reserved	reserved	reserved	reserved	reserved	reserved	reserved

Description:

- reserved: reserved, do not write

I2C Register (for temperatur sensor control)

Reading I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	SCL	SDA	1	1	1	1

Description:

- SDA: Data Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SCL: Clock Port Pin State
  0 = Pin State = Low
  1 = Pin State = High
- SDAO: Data Port Output Latch State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output State
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

Writing I/O Register 820Bh:

D7	D6	D5	D4	D3	D2	D1	D0
SCLO	SDAO	X	X	X	X	X	X

Description:

- SDAO: Data Port Output Latch
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)
- SCLO: Clock Port Output
  0 = Output Latch State = Low
  1 = Output Latch State = High (Open Collector)

4.3. Peripheral Devices

4.3.1. VGA-Interface

The VGA interface uses the standard PC/AT VGA register set. For detailled programming information please refer to the IBM PC/AT Technical Reference or similar documentation.
Low level programming is handled by the VESA compatible VGA-BIOS.
This interface is not available on NETIPC-6AD.

4.3.2. IDE-Interface

The IDE interface uses the standard PC/AT register set. For detailled programming information please refer to the IBM PC/AT Technical Reference, ATA/ATAPI standards (ANSI) or similar documentation.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit FIFOs. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation.

4.3.4. Keyboard/Mouse Interface

The Keyboard/Mouse interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 82C42 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.5. Ethernet Interface

On the NETIPC-6A board the Ethernet interface uses the Intel 82551 Ethernet Controller. For detailed programming information and drivers check www.syslogic.ch and www.intel.com .

4.3.6. Temperature Sensor

The Temperator Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the NETIPC. The LM75 can be accessed at the I2C address 00h. For detailled programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.
Poweron default setting for OVERTMP* is 80°C chip temperature.

I2C Address	Device	Remarks
00h	LM75	

Tab. 27 I2C Address Space

4.3.7. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.
If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the NETIPC Setup Register.
The watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the NETIPC Control Register. The application must check the WDG* bit in the NETIPC Status Register uppon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the NETIPC Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.
Sample code showing the initialisation and triggering of the watchdog is available in the free IPC/IOCOMSW-1A package.
For watchdog support on the BIOS level please consult the NETIPCFW firmware documentation. In this case initialisation is done by the BIOS on startup and triggering is done through BIOS API INT 15h calls.

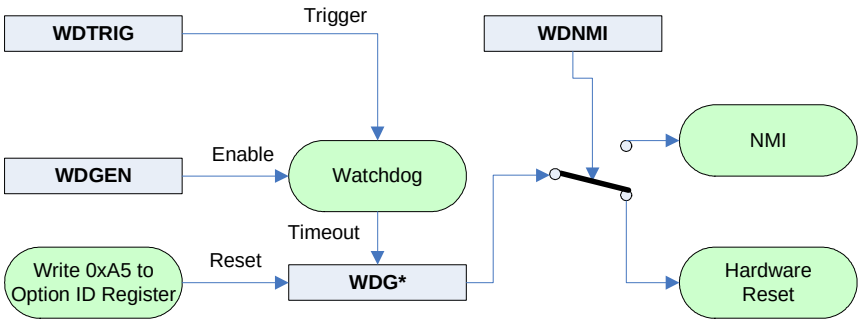

Fig. 9 Watchdog Blockdiagram

The watchdog can only initiate a hardware reset. The NMI option is not supported.

4.3.8. PC/104 Bus Interface

For detailed description of PC/104 add-on board programming please consult PC/104 and ISA bus standard documentation and related PC/AT architecture literature as well as the add-on boards documentation.

5 Technical Data

5.1. Electrical Data

Important Note

Do not operate the NETIPC board outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		1500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		1000			Vdc
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to PC/104 mounting holes		0.5			mm
RJ45 to logic		2.5			mm
RJ45 to chassis and PCB boarder		2.0			mm
storage temperature range	Tst	-40		90	°C

Tab. 28 General Absolute Maximum Ratings

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
internal logic supply voltage	Vcc	4.75	5.00	5.25	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.70	3.00	3.60	Vdc
PS/2 connector (P3/P4) power load (+5V)	Ips2			200	mA
operating free-air temperature range (standard products)	Ta	0		70	°C

Tab. 29 General Recommended Operating Conditions

Electrical Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	Typ	max	Unit
IPC/NETIPC-6L(N) specific electrical characteristics					
logic supply current (Vcc=5V, no external loads)	Icc		0.95	1.07	A
full load power dissipation (worst case)	Pmax		4.75	5.35	W
IPC/NETIPC-6A(N) specific electrical characteristics					
logic supply current (Vcc=5V, no external loads)	Icc		1.22	1.30	A
full load power dissipation (worst case)	Pmax		6.1	6.5	W
IPC/NETIPC-6H(N) specific electrical characteristics					
logic supply current (Vcc=5V, no external loads)	Icc		tbd	tbd	A
full load power dissipation (worst case)	Pmax		tbd	tbd	W
Applies to all IPC/NETIPC-6 derivates					
Vbatt loading (Vcc=0V, without SocketMemory)	Ibat(off)		3.5	10.0	uA
Vbatt loading (Vcc=5V)	Ibat(on)		1.5	4.0	uA
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			2		V
AC97 Line In			1		Vrms
AC97 Mic In			1		Vrms
AC97 Line Out		0.85	1	1.15	Vrms

Tab. 30 General Electrical Characteristics

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
IPC/NETIPC-6L(N) specific switching characteristics					
processor clock	pclk			433	MHz
memory clock (DDR333)	mclk			167	MHz
IPC/NETIPC-6A(N) specific switching characteristics					
processor clock	pclk			500	MHz
memory clock (DDR400)	mclk			200	MHz
IPC/NETIPC-6H(N) specific switching characteristics					
processor clock	pclk			600	MHz
memory clock (DDR400)	mclk			200	MHz
Applies to all IPC/NETIPC-6 derivates					
COM1/2 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock 1	fclk1		14.318		MHz
Timer base clock 1 accuracy				+/-100	ppm
Timer base clock 2	fclk2		32.768		kHz
Timer base clock 2 accuracy				+/-20	ppm
Timer base clock 2 aging				+/-3	ppm/year
Real Time Clock base clock	fclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year
AC97 Sampling rate				48	kHz
AC97 DAC dynamic range		85			dB
AC97 ADC dynamic range		80			dB

Tab. 31 General Switching Characteristics

5.2. Mechanical Data

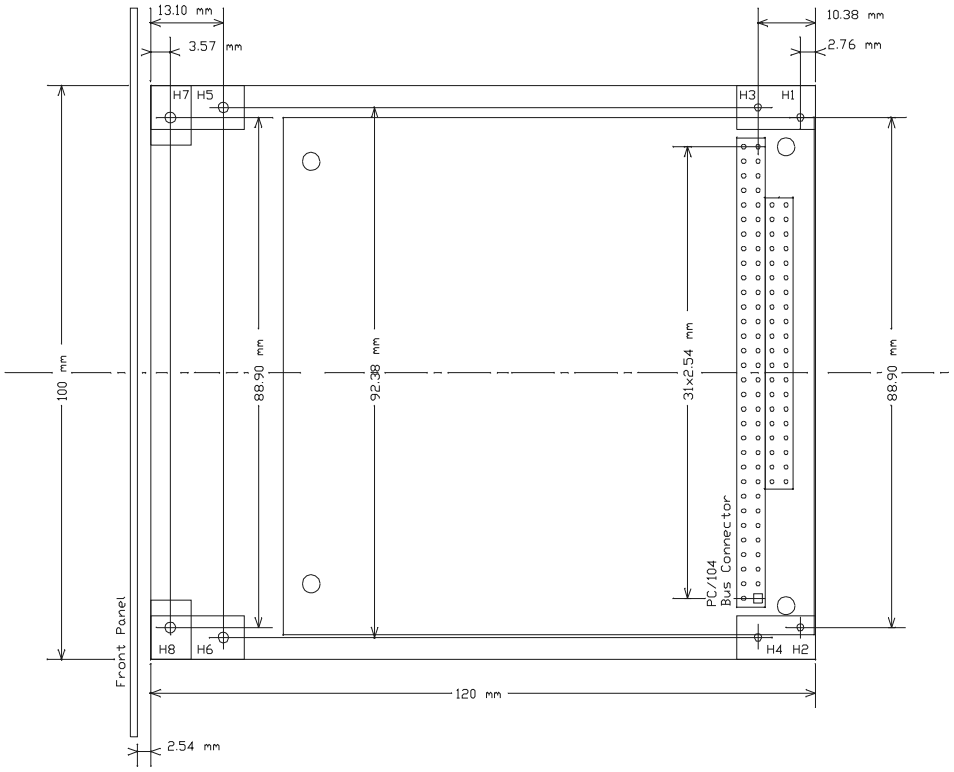

Fig. 10 Mechanical Outline

5.3. EMI / EMC Specification

5.3.1. Relevant Standards

The IPC/NETIPC-6 has been designed to comply the the following standards:

- EN 55022 Information technology equipment-
  Radio disturbance characteristics-
  Limits and methods of measurement

- EN 55024 Information technology equipment-
  Immunity characteristics -
  Limits and methods of measurement

- EN 61000-6-2 Electromagnetic compatibility (EMC),
  Part 6-2: Generic standards- Immunity for industrial environments

- EN 61000-6-4 Electromagnetic compatibility (EMC), Part 6-4: Generic standards – Emission standard for industrial environments

5.3.2. Emission

No testing has been done on board level. However the board has been tested in a complete systems (including power supply, enclosure, additional boards). Please refer to the appropriate product documentation for more details.

5.3.3. Immunity

No testing has been done on board level. However the board has been tested in a complete systems (including power supply, enclosure, additional boards). Please refer to the appropriate product documentation for more details.

5.4. Environmental Specification

No testing has been done on board level. However the board has been tested in a complete systems (including power supply, enclosure, additional boards). Please refer to the appropriate product documentation for more details.

6 Firmware

6.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System

  Note : Refer to the BIOS documentation for detailled information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs

  Note : Refer to the OS documentation for detailled information

Application Programs

- Initialization of NETIPC system, communications and external devices
- Start procedure for the Control Tasks

  Note : Refer to the Application Programs documentation for detailled information

6.2. Firmware Functions

The NETIPC board is setup with the firmware IPC/NETIPCFW-6A (see documentation DOC/NETIPCFW6 for details). Some standard PC/AT peripheral devices (e.g. VGA, Keyboard/Mouse, Serial Ports, IDE interface) are directly supported by the BIOS, BIOS extensions and Operating Systems. Some peripheral devices are directly supported by standard communication software (e.g. TCP/IP stacks, TCP packet drivers) others need special programming according to the freely available sample software IPC/IOCOMSW6-1A (e.g. Watchdog). Please refer to the appropriate documentation for detailed information.

6.3. Application Programming Interface (API)

The NETIPC board does not contain any special API besides the installed BIOS and DOS. Refer to the BIOS and Operating System documentation (included in DOC/NETIPCFW6) for API specifications.

6.4. Operating Systems

Syslogic offers an implementation for the following operting systems (OS):

Debian Linux Distribution
IPC/DEBIAN-40A

Microsoft Windows CE 5.0
IPC/WINCE-50A

Microsoft Windows XP Embedded
IPC/WINXPE-6A

Others on request.

Important Note

When implementing a BSP for a new OS be sure to use the “Pentium Platform”.

7 Product Revision History

7.1. Hardware

This paragraph lists the different hardware revisions of the NETIPC boards delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Logic Revision ID Register	Remarks
IPC/NETIPC-6L(N)	#1	11h	Original Release, RoHS compliant
IPC/NETIPC-6L(N)	#1	10h	Watchdog support added
IPC/NETIPC-6A(N)	#1	10h	Original Release, RoHS compliant
IPC/NETIPC-6A(N)	#2	11h	IRQ fixed
IPC/NETIPC-6A(N)	#3	12h	New PCI/ISA Bridge (IT8888)
IPC/NETIPC-6A(N)	#3	13h	Watchdog support added
IPC/NETIPC-6H(N)	#0	00h	Prototype / Engineering Sample

Tab. 32 Hardware Revision State

7.2. Firmware

Please refer to the firmware documentation DOC/NETIPCFW6 for detailed information.

Important Note

This document always covers the latest product revision listed in Tab. 32.
Please contact the manufacturers technical support for upgrade options.

8 Manufacturer Information

8.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Täfernstrasse 28
CH-5405 Baden-Dättwil / Switzerland

Email: info@syslogic.ch
www: http://www.syslogic.ch
Phone +41 (0)56 200 90 40
Fax: +41 (0)56 200 90 50

Technical support:
support@syslogic.ch