IPC/S41F08-AxxxE, IPC/M41F08-AxxxE

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1.0	12.01.2014	U. Müller	
1.1	26.01.2015	U. Müller	typo corrections
1.2	05.06.2015	U. Müller	added battery service information
1.3	08.06.2017	U. Müller	added isolation voltage spec for CAN, RS485

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1 Introduction

1.1. General Remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.
Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.
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CFast	trademark of SanDisk Corporation
PC/104	trademark of PC/104 Consortium

1.2. Contents of this Documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the PC/104 system. It provides all information needed to configure, setup and program the IPC/M41F08-AxxxE systems. For complete information also the documentation of the mounted communications and I/O boards must be consulted. In the following paragraphs all descriptions referenced to M41F08 apply to all, the IPC/M41F08-AxxxE and IPC/S41F08-AxxxE products, if not declared otherwise.

1.3. Additional Products and Documents

1.3.1. Hardware Products

The following hardware products are useful together with the M41F08 system:
- Syslogic PC/104 communication boards (see product catalog)
- Syslogic PC/104 I/O boards (see product catalog)

1.3.2. Software Products

The following software products are useful together with the M41F08 system:
- IPC/IOCOMSW-1A: Sample program code and utilities for x86 based PC/104 systems

1.3.3. Documents

The following additional documents are *useful* for correct installation and operation of the M41F08 system:

- DOC/IPC_IOCOMSW: User Documentation for programming examples and utilities

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
- IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'
- ISBN 0-929392-15-9: 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego)

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org
- Global Engineering Documents
  www.global.ihs.com

1.4. Items delivered

The M41F08 comes without external cabling and power supply. These additional items must be ordered separately and installed according to the respective user documentations.

1.5. Installation

The installation of the M41F08 system is described in chapter 5 of this documentation.

Important Note

Before applying power to the M41F08 system, all installed boards must be correctly configured and mounted.

1.6. Safety Recommendations and Warnings

1.6.1. General safety recommendations

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.
The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.
The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.
In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 10). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

1.6.2. Safety warnings

Do not operate this product outside of the recommended operating conditions according to the technical data specified in paragraph 6.

Do not touch the surface of this product without precaution, it may be hot and burn your skin. Cool it down before touching.

Do not touch any connector unless you have verified that no dangerous voltage is around. Disconnect cabling first.

Do not open any part of the enclosure while power is applied.

Do not try to repair any defective product by yourself. There is no replaceable service part inside.

Do not open the service cover unless you are instructed and entitled to do this. The service cover is intended for inserting the CFast Software storage card on initial operation of the product by an instructed person only.

Use an overload protected power supply to prevent damage in case of a short inside the system.

1.7. Electro-static discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in a ESD protected environment. Otherwise a proper operation is not guaranteed and the warranty is not applicable.

1.8. Life Cycle Information

1.8.1. Transportation and Storage

During transportation and storage the products must be in their original packing. The original packing contains an antistatic bag and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.8.2. Assembly and Installation

Observe the EMI-precautions against static discharge. Carefully read the assembly and installation documentation (see chapter 5) before unpacking the products. Make sure that you have all the necessary items ready (including all the small parts). Follow the assembly guidelines in chapter 5 strictly.
The installation procedures must be strictly observed. Note that deviations from the installation guidelines may result in degraded operational reliability or in unfavourable EM-radiation or EM-susceptibility.

1.8.3. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.
The main functionality of the M41F08 system is defined by the application programs running on the processor board. The application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.8.4. Maintenance and Repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (EMI and mechanical protection).

1.8.5. Disposal

At the end of the lifespan the M41F08 products must be properly disposed. M41F08 products contain a multitude of elements and must be disposed like computer parts. Some of the M41F08 products contain batteries which should be properly disposed.

2 Product Description

2.1. Features

The M41F08 system is a x86 based industrial PC designed for use with the IPC line of communications and I/O boards. Its many different variants allow to build up various industrial controls based on the standard PC/AT architecture.
The M41F08 offers the following main features:

- low power industrial processor board eliminating the need for enforced cooling
- high performance 32-bit 6-stage pipeline 486 based processor core with integrated floating point unit
- 800 MHz processor clock
- DDR2 DRAM interface
- 1 Gbyte DRAM on board
- 64-bit graphics controller with backwards compatibility to VGA and SVGA standards
- CRT controller supporting up to 1280 x 1024 dots resolution
- LCD interface (3x6 bit CMOS)
- SATA interface supporting one CFast card socket.
- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- PC/AT compatible keyboard controller (8042)
- up to four serial RS232 ports (COM1-4) with 16 byte receive and transmit fifo (16550A)
- option of up to two of the serial ports (COM3, 4) as galvanic isolated RS422/485 interfaces (half/fullduplex)
- up to four USB V2.0 ports (OHCI/EHCI-Hostcontroller) with High-, Full- and Low-Speed support
- up to two Ethernet LAN interface (one 10/100Mbit, one 10/100/1000Mbit)
- Year 2000 compliant Real Time Clock (PC/AT compatible)
- hardware watchdog configurable for 100 ms or 1.6 s timeout and Non-maskable Interrupt (NMI) or hardware reset activation
- temperature supervisor for software controlled power management
- 16 Mbit BootBlock Flash for BIOS and BIOS extensions
- supervised battery backup for Real Time Clock
- PC/104 bus interface for expansion with standard 8/16 bit PC/104 communications and I/O boards

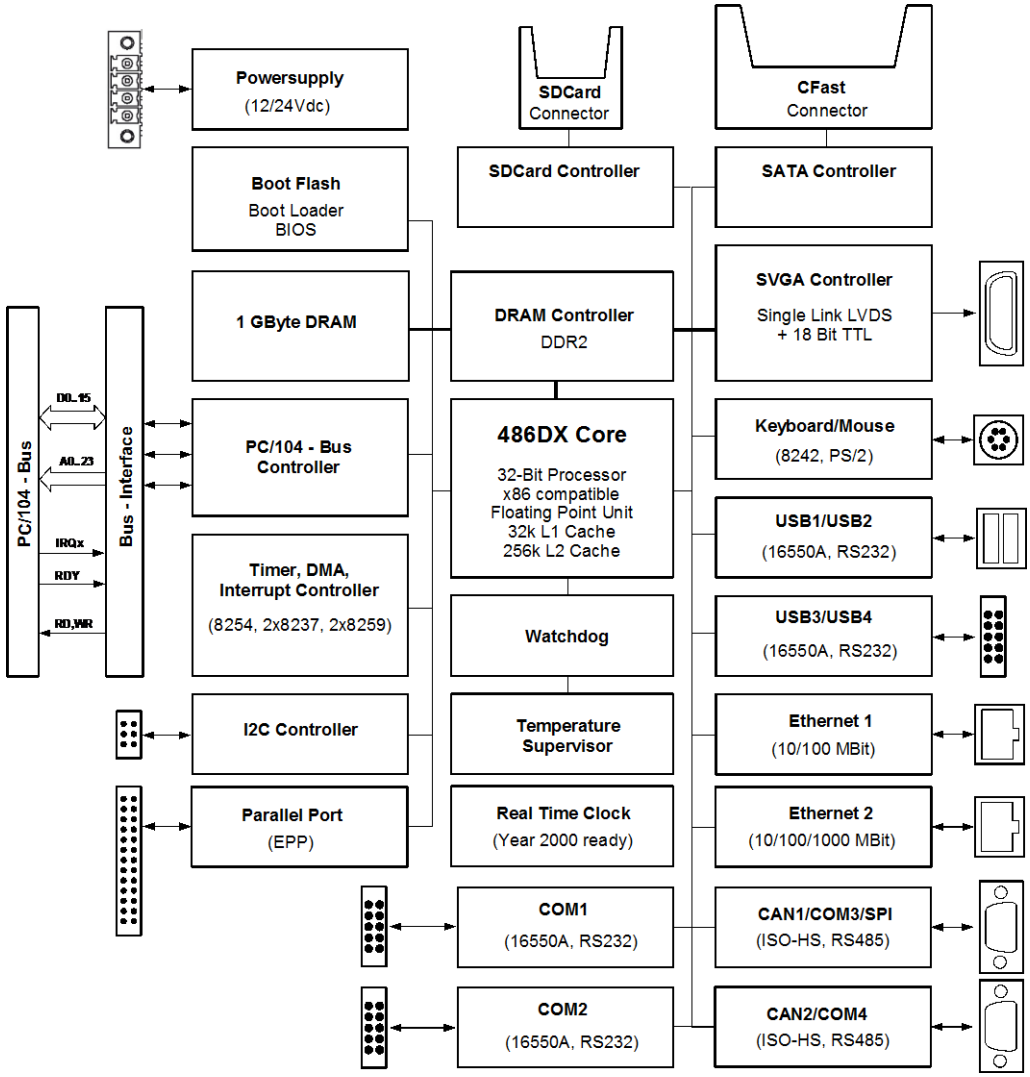

Fig. 1 Block Diagram M41F08 (all functions)

Important Note

Check the product variant carefully for the supported functions.

2.2. Product Variants

The M41F08 is available in many different functional variants and enclosures.
The following tables show the functional differences for the M size enclosure and the S size enclosure variants. Bold printed functions are available on a front or rear connector, italic printed functions are available as internal interfaces only. See figure Fig. 2 for location of the internal interfaces.

Function	IPC/S41F08-A101E	IPC/S41F08-A102E	IPC/S41F08-A103E	IPC/S41F08-A104E
LAN1	**ETH1**	**ETH1**	**ETH1**	**ETH1**
LAN2	**ETH2**	**ETH2**	**ETH2**	**ETH2**
COM1	*P41/RS232*	*P41/RS232*	*P41/RS232*	**X1/RS232**
COM2	*P42/RS232*	*P42/RS232*	*P42/RS232*	**X2/RS232**
COM3	*P43/RS232*	*P43/RS232*	**X1/RS485**	*P43/RS232*
COM4	**X2/RS485**	*P44/RS232*	**X2/RS485**	*P44/RS232*
CAN1	**X1**	**X1**	-	-
CAN2	-	**X2**	-	-
USB0/1	**USB0/1**	**USB0/1**	**USB0/1**	**USB0/1**
USB2/3	*P22*	*P22*	*P22*	*P22*
LPT1	*P45*	-	-	-
PS/2 Keyb	*P4*	*P4*	*P4*	*P4*
VGA	**VGA**	**VGA**	**VGA**	**VGA**
LCD TTL	*P30*	*P30*	*P30*	*P30*
LCD LVDS	*P32*	*P32*	*P32*	*P32*
LCD Backlight	*P31/5V*	*P31/5V*	*P31/5V*	*P31/5V*
I2C	*P46*	*P46*	*P46*	*P46*
CFast	*P8*	*P8*	*P8*	*P8*
SDCard	*P7*	-	-	-
PC/104 Slot	-	-	-	-
RTC Backup	GoldCap	Li battery	GoldCap	GoldCap

Tab. 1 Product Variants S

Function	IPC/M41F08-A101E	IPC/M41F08-A102E	IPC/M41F08-A103E	IPC/M41F08-A104E
LAN1	**ETH1**	**ETH1**	**ETH1**	**ETH1**
LAN2	**ETH2**	**ETH2**	**ETH2**	**ETH2**
COM1	**X3/RS232**	**X3/RS232**	**X3/RS232**	**X1/RS232**
COM2	*P42/RS232*	**X4/RS232**	**X4/RS232**	**X2/RS232**
COM3	*P43/RS232*	*P43/RS232*	**X1/RS485**	**X3/RS232**
COM4	**X2/RS485**	*P44/RS232*	**X2/RS485**	**X4/RS232**
CAN1	**X1**	**X1**	-	-
CAN2	-	**X2**	-	-
USB0/1	**USB0/1**	**USB0/1**	**USB0/1**	**USB0/1**
USB2/3	*P22*	*P22*	*P22*	*P22*
LPT1	**LPT**	-	-	-
PS/2 Keyb	*P4*	*P4*	*P4*	*P4*
VGA	**VGA**	**VGA**	**VGA**	**VGA**
LCD TTL	*P30*	*P30*	*P30*	*P30*
LCD LVDS	*P32*	*P32*	*P32*	*P32*
LCD Backlight	*P31/5V*	*P31/5V*	*P31/5V*	*P31/5V*
I2C	*P46*	*P46*	*P46*	*P46*
CFast	*P8*	*P8*	*P8*	*P8*
SDCard	*P7*	-	-	-
PC/104 Slot	yes	yes	yes	yes
RTC Backup	GoldCap	Li battery	GoldCap	GoldCap

Tab. 2 Product Variants M

2.3. Operating Modes

The M41F08 is based on the standard PC/AT architecture and therefore operates in DOS-compatible mode (real mode) on start up. The configurable BIOS initializes all onboard peripherals to theire default values, executes the BIOS extensions programmed into the onboard BIOS-Flash and BIOS extensions found on installed expansion boards prior to booting the operating system from a user-selectable drive (boot sector). The operating system (or eventually a BIOS extension) may switch to protected mode to execute high performance 32-bit program code.

2.4. Startup Modes

The M41F08 may startup either in normal operating mode or in BIOS recovery mode:

- BIOS recovery mode is invoked when rotary switch S1 is set to position ‘8’. In BIOS recovery mode a corrupt BIOS may be reprogrammed.
- Normal operating mode is invoked when rotary switch S1 is set to position ‘0’.

3 Hardware Description

3.1. Overview

The M41F08 hardware may be configured by software (CMOS setup) and by switch settings. Custom BIOS configuration can be programmed into the BIOS flash on request (ask Syslogic technical support for custom BIOS configuration).
The switch and connector locations are shown in the board layout drawing (Fig. 2).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

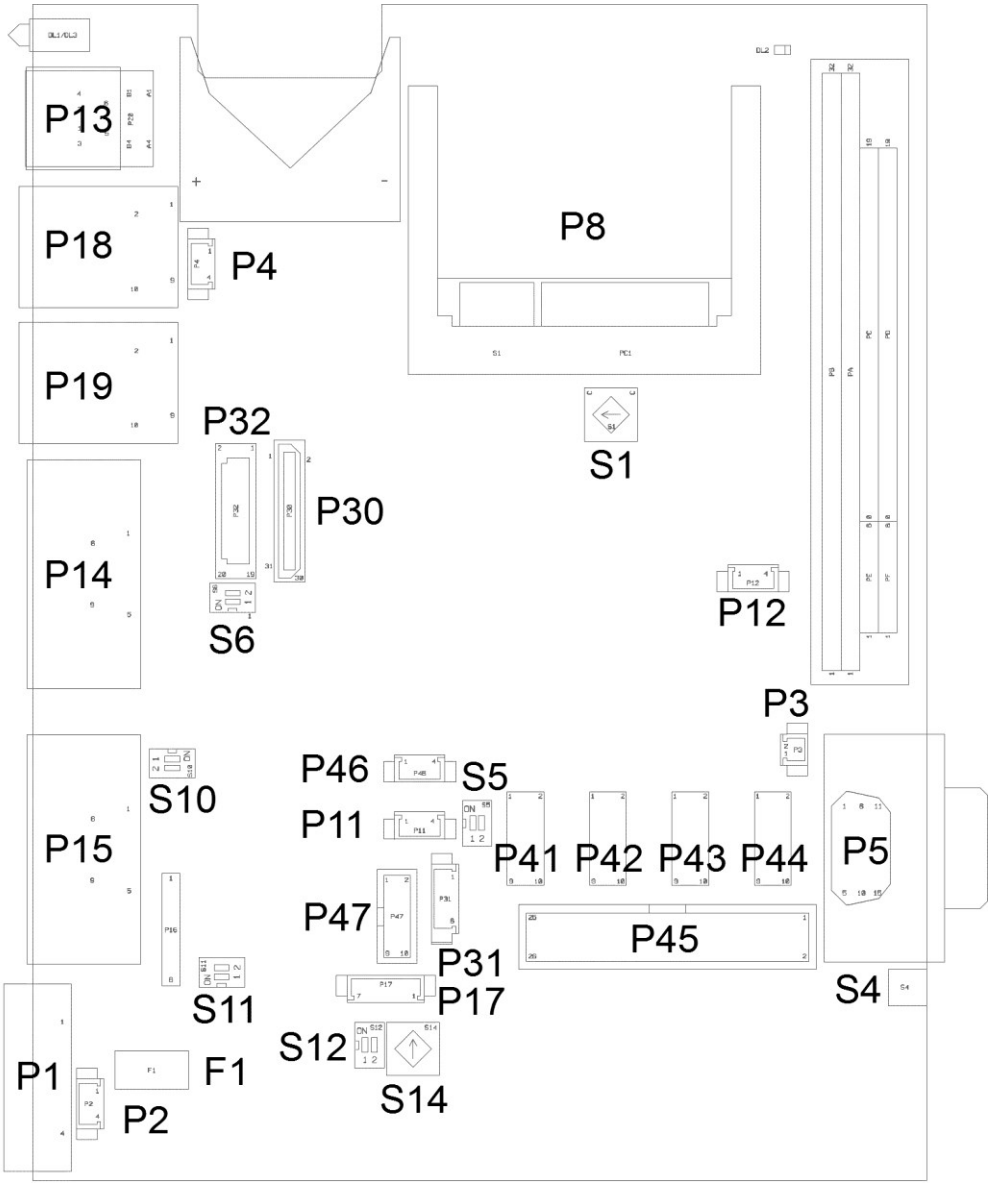

Fig. 2 Board Layout M41F08 (all functions)

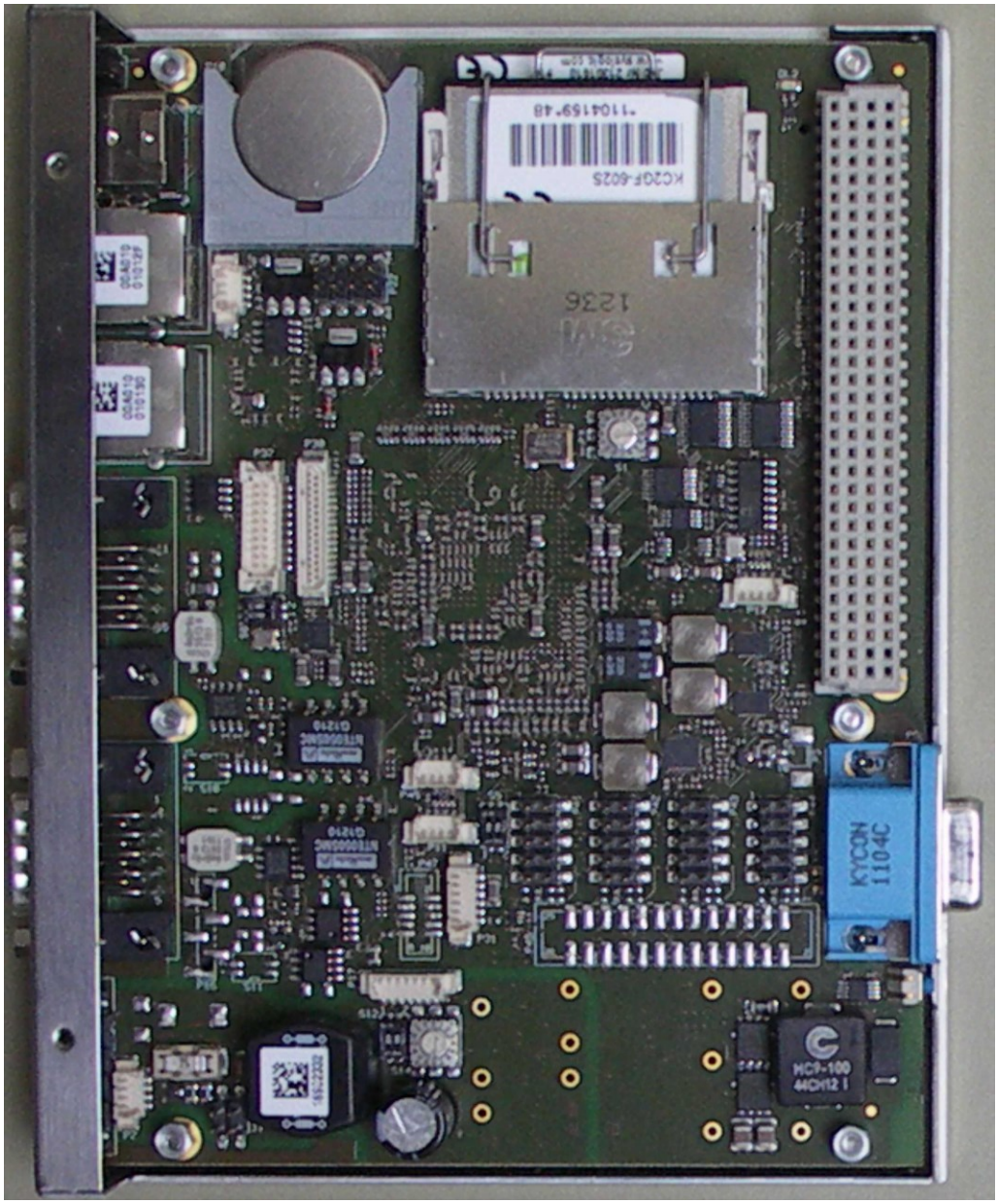

Fig. 3 Board Top View (IPC/S41F08-A102E)

3.2. Memory and I/O Resources

3.2.1. General Memory Layout and Configuration

The M41F08 uses the same memory layout as a standard desktop PC. Three onboard devices , DRAM, graphics controller, and BIOS flash, make use of the 4 Gbyte adressable memory space.

Address	Device / Register	Remarks
0000'0000..0009'FFFFH	640 kbyte Main Memory (DRAM)	
000A'0000..000B'FFFFH	VGA Video Memory	
000C'0000..000F'FFFFH	Configurable memory range (BIOS, BIOS Extensions, DRAM or redirected to PC/104 bus)	
0010'0000..3DFF'FFFFH	991 Mbyte Main Memory (DRAM)	
3E00'0000..3FFF'FFFFH	32 Mbyte Graphics Memory (DRAM)	UMA, do not access
4000'0000..83EF'FFFFH	reserved	do not access
83E0'0000..83FF'FFFFH	2 Mbyte BIOS Flash (mirrored)	do not access
8400'0000..FFFF'FFFFH	reserved	do not access
FFE0'0000..FFFF'FFFFH	2 Mbyte BIOS Flash	do not access

Tab. 3 Physical Memory Address Space Layout

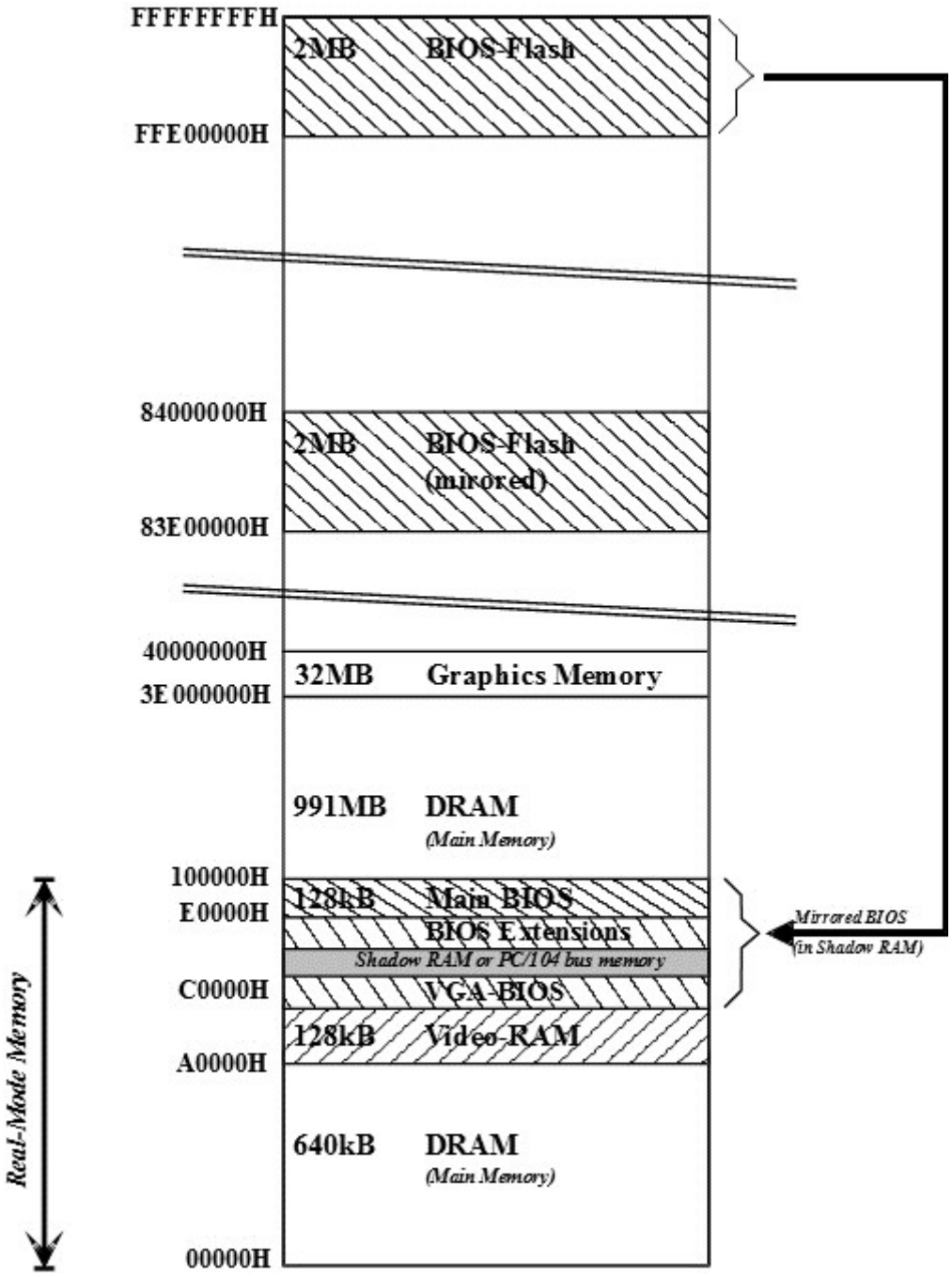

Fig. 4 Memory Map

3.2.2. General I/O Layout and Configuration

The M41F08's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address	Device / Register	Remarks
0000..001FH	DMA Controller 1	
0020..0021H	Master Interrupt Controller	
0022H	Configuration Address Register	
0023H	Configuration Data Register	
0024..003FH	reserved	
0040..0043H	Timer/Counter	
0044..005FH	reserved	
0060H	Keyboard/Mouse Controller	
0061H	Port B Register	
0062..0063H	reserved	
0064H	Keyboard/Mouse Controller	
0065..006FH	reserved	
0070H	Bit 6..0 = RealTimeClock/CMOS-RAM Address Register Bit 7 = Non Maskable Interrupt (NMI) Mask (write only)	
0071H	RealTimeClock/CMOS-RAM Data Register	
0072..007FH	reserved	
0080..0091H	DMA Page Registers / reserved	
0092H	Port 92h System Control Register	
0093..009FH	reserved	
00A0..00A1H	Slave Interrupt Controller	
00A2..00BFH	reserved	
00C0..00DFH	DMA Controller 2	
00E0..00FFH	reserved	
0100..016FH	not used	
0170..0177H	Secondary IDE Channel (SATA/CFast)	
0178..01EFH	not used	
01F0..01F7H	Primary IDE Channel (SDCard)	
01F8..0277H	not used	
0278..027FH	reserved for Parallel Port (LPT2) and Plug'n Play	
0280..02E7H	not used	
02E8..02EFH	Serial Port (COM4)	
02F0..02F7H	not used	
02F8..02FFH	Serial Port (COM2)	
0300..036FH	not used	
0370..0377H	reserved for external Secondary Floppy Controller	
0376..0377H	reserved for external Secondary IDE Channel	
0378..037FH	reserved for Parallel Port (LPT1)	
0380..03AFH	not used	

03B0..03BBH	VGA registers (MDA)	
03BC..03BFH	reserved for Parallel Port (LPT3)	
03C0..03CFH	VGA registers (EGA)	
03D0..03DFH	VGA registers (CGA)	
03E0..03E7H	not used	
03E8..03EFH	Serial Port (COM3)	
03F0..03F7H	reserved for external Primary Floppy Controller	
03F6..03F7H	Primary IDE Channel	
03F8..03FFH	Serial Port (COM1)	
0400..042FH	reserved	
0430..04EFH	not used	
0480..048FH	DMA High Page Registers / reserved	
0490..049FH	Instruction Counter Registers / reserved	
04A0..04CFH	not used	
04D0..04D1H	IRQ Edge/Level Control	
04D2..04FFH	not used	
0500..08FFH	not used	
0900..0A77H	not used	
0A78H	Plug'n Play configuration port	
0A79..0BFFH	not used	
0C00..0CF7H	not used	
0CF8..0CFFH	PCI configuration registers	
0D00..0FFFH	not used	
1000..3FFFH	not used	
4000.. 46E7H	not used	
46E8H	reserved	
46E9..47FFH	not used	
4800..7FFFH	not used	
8000..81FFH	reserved	
8200..821FH	M41F08 system registers	
8220..83FFH	reserved for Syslogic IPC add-on boards	
8400..BFFFH	reserved	
C000..EFFFH	reserved for PCI devices (VGA, Ethernet, USB, IDE)	
F000..FFFFH	reserved	

Tab. 4 I/O Address Space Layout

The processor device on the M41F08 board is factory programmed using some pins of the internal header P11. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK (do not connect)	
2	TDO (do not connect)	
3	TMS (do not connect)	
4	TDI (do not connect)	

Tab. 5 Factory Programming Header P11 (1x4 pin)

The programmable logic device on the M41F08 board is factory programmed using some pins of the internal header P12. These pins **must not** be connected by the user.

Pin Number	Signal	Remarks
1	TCK (do not connect)	
2	TDO (do not connect)	
3	TMS (do not connect)	
4	TDI (do not connect)	

Tab. 6 Factory Programming Header P12 (1x4 pin)

The power management controller on the M41F08 board is factory programmed using the internal header P17. This header **must not** be connected by the user.

Pin Number	Signal	Remarks
1	VPP/MCLR# (do not connect)	PICkit3 pin 1
2	VCC (do not connect)	PICkit3 pin 2
3	GND (do not connect)	PICkit3 pin 3
4	PGD (ICSPDAT, do not connect)	PICkit3 pin 4
5	PGC (ICSPCLK, do not connect)	PICkit3 pin 5
6	PGM LVP (SCL, do not connect)	PICkit3 pin 6
7	-- (SDA, do not connect)	--

Tab. 7 Factory Programming Header P17 (1x7 pin)

3.3. Peripheral Devices

3.3.1. VGA Interface

The VGA signals are available on the High Density DSUB15 connector P5 for direct connection of VGA compatible monitors. The controller uses the standard VGA register interface. All configuration is done by software (BIOS, VGA-BIOS).

Device Connection

Pin Number	Signal	Remarks
1	RED	
2	GREEN	
3	BLUE	
4	-	
5	GND	
6	Analog GND	
7	Analog GND	
8	Analog GND	
9	+5V	not fused
10	GND	
11	-	
12	DDC Data	
13	HSYNC	
14	VSYNC	
15	DDC Clock	

Tab. 8 VGA connector P5 (DSUB15HD)

Important Note

Maximum cable length allowed for VGA connection is 15 m.
Use high quality shielded VGA cables (with coaxial wires for RGB signals) for maximum EMI protection.

3.3.2. LCD/LVDS-Interface

The LCD/LVDS interface is an optional interface for direct connection of an external TFT display. It supports 3.3V 6-bit CMOS TFT panels on connector P30 or 3.3V 6/8-bit LVDS TFT panels on connector P32. Direct inverter connection is provided through P31 if power requirement is not to high.
Note that special BIOS-Version are required for operation of the LCD/LVDS interface. Contact Syslogic technical support for details.

Device Connection (LCD-Panel)

Mating connector type: Hirose DF13-20DS-1.25C, Crimp contact DF13-3032SCF.

Pin Number	Signal	Pin Number	Remarks
1	VCC_LCD (3.3V)	2	VCC_LCD (3.3V)
3	GND	4	GND
5	LVDS0-	6	LVDS0+
7	GND	8	LVDS1-
9	LVDS1+	10	GND
11	LVDS2-	12	LVDS2+
13	GND	14	LVDSCLK0-
15	LVDSCLK0+	16	GND
17	LVDS3-	18	LVDS3+
19	FPMODE (S6 Slider 1) Mode control (off=1k pullup to 3.3V / on=ground)	20	FPHMODE (S6 Slider 2) Mode control (off=1k pullup to 3.3V / on=ground)

Tab. 9 LVDS connector P32 (Hirose DF13A-20DP-1.25V)

Important Note

Do not draw more than 1.0 Ampere from VCC_LCD (max. 0.5 Ampere per pin).
This interface is intended for case internal use only.

Device Connection (LCD-Panel)

Mating connector type: Hirose DF9-31S-1V.

Pin Number	Signal	Remarks
1	GND	Ground
2	DCLK	Clock signal for sampling catch data signal
3	HS	Horizontal sync signal
4	VS	Vertical sync signal
5	GND	Ground
6	R0	Red data signal (LSB)
7	R1	Red data signal
8	R2	Red data signal
9	R3	Red data signal
10	R4	Red data signal
11	R5	Red data signal (MSB)
12	GND	Ground
13	G0	Green data signal (LSB)
14	G1	Green data signal
15	G2	Green data signal
16	G3	Green data signal
17	G4	Green data signal
18	G5	Green data signal (MSB)
19	GND	Ground
20	B0	Blue data signal (LSB)
21	B1	Blue data signal
22	B2	Blue data signal
23	B3	Blue data signal
24	B4	Blue data signal
25	B5	Blue data signal (MSB)
26	GND	Ground
27	DEN	Data enable signal
28	VCC_LCD	Power supply 3.3V
29	VCC_LCD	Power supply 3.3V
30	HMODE (S6 Slider 2)	Mode control (off=1k pullup to 3.3V / on=ground)
31	VMODE (S6 Slider 1)	Mode control (off=1k pullup to 3.3V / on=ground)

Tab. 10 LCD connector P30 (Hirose DF9B-31P-1V)

Important Note

Do not draw more than 1.0 Ampere from VCC_LCD (max. 0.5 Ampere per pin).
This interface is intended for case internal use only

Device Connection (Inverter)

Mating connector type: Housing Molex 51021-0800, Crimp contact Molex 50058-8100.
Wiring: AWG26.

Pin Number	Signal	Remarks
1	VCC_INV	Inverter Power 5V
2	VCC_INV	Inverter Power 5V
3	GND	Ground
4	GND	Ground
5	EN	Inverter enable
6	LCD Brightness (0..5V)	Brightness Control

Tab. 11 Inverter connector P31 (Molex 53398-0871)

Important Note

Do not draw more than 1.0 Ampere from VCC_INV (max. 0.5 Ampere per pin).
Check inverter board datasheet for polarity of brightness control and other requirements.
This interface is intended for case internal use only.

3.3.3. Buzzer Interface

A standard buzzer interface is available on internal connector P3 for connection of a PC buzzer like TDK SD1209T5-A1 or similar type. The buzzer drive signal is generated by the standard PC timer 1 and buffered by an open collector NPN transistor.

Device Connection

Pin Number	Signal	Remarks
1	BUZ+ (5V)	not fused
2	BUZ- (buzzer drive signal)	100mA max

Tab. 12 Buzzer interface connector P3

Important Note

This interface is intended for case internal use only.

3.3.4. IDE/SATA/CFast-Interface

The Secondary IDE Channel hosts a SATA controller which serves the CFast socket P8. It uses the standard PC IDE address decoding when operated in legacy mode.
The CFast card behaves like a standard IDE disk or IDE CompactFlash.

Tested CFast cards are:

- Cactus Technologies KC-series

Device Connection

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Pin Number	Signal	Pin Number	Signal
S1	SGND	PC1	CDI
S2	RxP	PC2	GND
S3	RxN	PC3	nc
S4	SGND	PC4	nc
S5	TxN	PC5	nc
S6	TxP	PC6	nc
S7	SGND	PC7	GND
		PC8	LED1
		PC9	LED2
		PC10	IO1
		PC11	IO2
		PC12	IO3
		PC13	PWR
		PC14	PWR
		PC15	PGND
		PC16	PGND
		PC17	CDO

Tab. 13 CFast Connector P8

Important Note

Do not insert or remove the CFast card when power supply is on. This interface does not support hot-plugging.

3.3.5. Serial Ports

Up to four serial ports are available with standard RS232 signals. Up to two of them can be used for full or half duplex RS485 communication (COM3, COM4).
The serial ports have fixed base addresses of 3F8H for COM1, 2F8H for COM2, 3E8H for COM3 and 2E8H for COM4.
COM1 uses hardware interrupt 4, COM2 uses hardware interrupt 3, COM3 uses hardware interrupt 10 and COM4 uses hardware interrupt 5.

Device Connection RS232

The Serial Port COM1 is available on the internal header P41.
The Serial Port COM2 is available on the internal header P42.
The Serial Port COM3/RS232 is available on the internal header P43.
The Serial Port COM4/RS232 is available on the internal header P44.

Pin Number	Signal	Pin Number	Signal
1	DCD*	2	DSR*
3	RXD	4	RTS*
5	TXD	6	CTS*
7	DTR*	8	RI*
9	GND	10	+5V (not fused)

Tab. 14 Serial Ports COM1-4 internal Headers P41-44 (2x5 pin)

Configuration Options RS485 (COM3, COM4 only)

Switch	Configuration	Remarks
S10: 1	OFF = COM3 full duplex RS485 ON = COM3 half duplex RS485	
S10: 2	don't care	
S11: 1	OFF = COM4 full duplex RS485 ON = COM4 half duplex RS485	
S11: 2	don't care	

Tab. 15 RS485 Configuration Options

Device Connection RS485 (COM3, COM4 only)

The Serial Port COM3/RS485 is available on connector P14.
The Serial Port COM4/RS485 is available on connector P15.
120 Ohm termination resistors must be connected externally!

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	RX-	7	RX+
3	TX-	8	TX+
4	no connection	9	no connection
5	RGND		

Tab. 16 Full duplex RS485 ports COM3, COM4 on DSUB-9 male P14, P15 (9 pin)

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	no connection	7	no connection
3	DATA-	8	DATA+
4	no connection	9	no connection
5	RGND		

Tab. 17 Half duplex RS485 ports COM3, COM4 on DSUB-9 male P14, P15 (9 pin)

3.3.6. Keyboard Interface

The keyboard signals are available on connector P4 for connection of PS/2 style keyboards. The controller uses hardware interrupt 1 for the keyboard.

Device Connection

Pin Number	Signal	Remarks
1	+5V (not fused)	
2	KBDATA	
3	KBCLK	
4	GND	

Tab. 18 PS/2 Keyboard connector P4

Important Note

Maximum cable length allowed for keyboard connection is 3 m.
Use shielded cables for maximum EMI protection.

3.3.7. USB Interface

The M41F08 features an OHCI/EHCI compatible USB hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS.

Device Connection

The USB interface uses a standard A type USB connector on the front for USB channels 0 and 1. Channels 2 and 3 are located on two parallel 4pin headers.

P22A Pin Number	USB channel 2 Signal	P22B Pin Number	USB channel 3 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 19 USB Interface Connector P22 (1x4pin/1x4pin)

Important Note

Maximum cable length allowed for USB connection is 3 m. If longer cables are used, special overvoltage and filtering elements have to be installed to comply with the requirements of EMI/RFI "CE"-certification. Only use high quality industrial USB devices with sufficient EMI compatibility.
Use shielded cables for maximum EMI protection.

3.3.8. CAN Interfaces

Up to two CAN 2.0b interfaces using standalone NXP SJA1000 CAN controllers.
CAN1 i/o base address 0x7600, IRQ11.
CAN2 i/o base address 0x7700, IRQ11 (shared).
Termination resistors must be added externally!

Pin Number	Signal	Pin Number	Signal
1	no connection	6	no connection
2	CAN Low	7	CAN High
3	CAN Ground	8	no connection
4	no connection	9	no connection
5	no connection		

Tab. 20 CAN port CAN1, CAN2 on DSUB-9 male P14, P15 (9 pin)

3.3.9. Ethernet LAN Interface

The M41F08 features up to two PCI Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. The Ethernet interface drives two LED's (yellow and green) integrated into the RJ45 connector for status information. The meaning of the LED activity is programmable (normally set by the low level driver).
LAN1 features a DMP/RDC RD6040 controller supporting 10/100Mb/s, LAN2 features an Intel 82574 controller supporting 10/100/1000Mb/s. Both interfaces support Auto Negotiation and Auto MDIX functions. Check manufacturer's datasheets for detailed information.
No configuration options are available for the Ethernet device.

Device Connection LAN1

The first Ethernet interface uses the standard RJ45 connector P18 on the front for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 21 Ethernet Twisted Pair Interface Connector P18 (RJ45)

Device Connection LAN2

The second Ethernet interface use the standard RJ45 Gigabit connector P19 on the front for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	MD0+	
2	MD0-	
3	MD1+	
4	MD2+	
5	MD2-	
6	MD1-	
7	MD3+	
8	MD3-	

Tab. 22 Ethernet Twisted Pair Interface Connector P19 (RJ45)

3.3.10. I2C Interface

The M41F08 features one I2C interface on an internal connector and another one on the PC/104 bus expansion rows F/E (see paragraph 3.3.16 for details). The interfaces are integrated into the Vortex86DX2 processor's South Bridge as PCI peripherals I2C0 and I2C1 (see processor datasheet for details). Both interfaces are non buffered 3.3V LVTTL interfaces with integrated pullups.
Consult processor datasheet for programming details.

Device Connection I2C0

The first I2C interface uses connector P46. Mating connector type: Housing Molex 51021-0400, Crimp contact Molex 50058-8100. Wiring: AWG26.

Pin Number	Signal	Remarks
1	VCC (3.3V)	not fused!
2	SDA	3.3V LVTTL with integrated pullup
3	SCL	3.3V LVTTL with integrated pullup
4	GND	

Tab. 23 I2C Interface Connector P46

Important Note
This interface is intended for case internal use only.

3.3.11. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the NETIPC's hardware reset or the processors NMI line depending on software configuration.

Configuration Options

Switch	Configuration	Remarks
S1	position '0' = 1.6 s position '1' = 100 ms	

Tab. 24 Watchdog Configuration Options

3.3.12. Power supply

The processor and its peripherals are powered by a non-isolated, integrated power supply which generates all the necessary voltages.
The power must be connected using the following mating connector:
Weidmueller BCZ 3.81/04/180F SN SW (Ordercode 1792970000).
The mating connector can be ordered directly at your local Weidmueller distributor .

Pin Number	Signal	Remarks
1	+24VDC_AUX	Auxiliary power supply
2	Power Fail/Remote on/off	Power fail input
3	+24VDC	+9V..+30V DC
4	GND	

Tab. 25 Power supply connector

For normal operation the external power supply has to be connected to the pins 3 (+24VDC) and 4 (GND) of the connector.
Pin 1 (+24VDC_AUX) may be used as a standby supply for the GoldCap RTC backup.
Pin 2 is used as an input for either a power fail or remote on/off signal.

3.3.13. Power supervision

The power management control unit (PCU) can be operated in two modes: power fail mode or remote on/off mode. The following two chapters describe their functionality in detail.

Switch	Configuration	Remarks
S12: 1 / 2	on / off = remote on/off mode off / on = power fail mode	check chapter 3.3.14/3.3.15

Tab. 26 Power supply configuration

Switch	Configuration	Remarks
S14	position ‘0’ = bypass mode (for power fail mode) position ‘1’ to ‘F’ = remote on/off mode	check chapter 3.3.14/3.3.15

Tab. 27 Power supply configuration

3.3.14. Power Fail

In power fail mode the microcontroller monitors the external power fail signal. The state of power fail signal can be access through the status register, I/O 8200h.

Application example

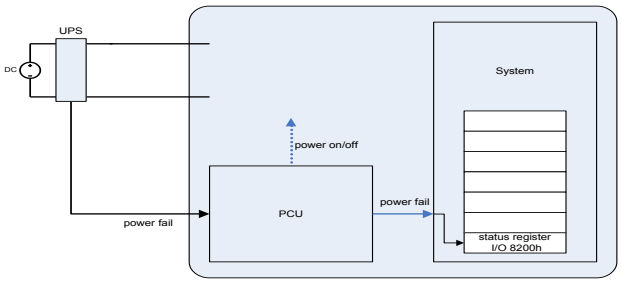

Fig. 5 Typical power fail application

The application has to poll the power fail flag and call different functions according to the state of the flag.

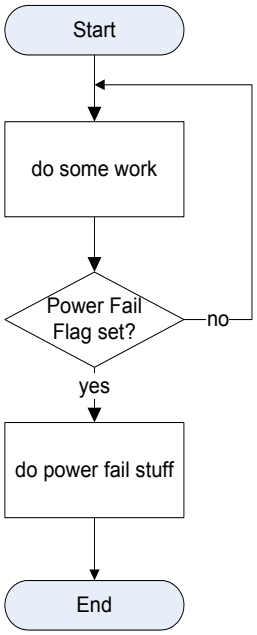

Fig. 6 Typical power fail flow

3.3.15. Remote On/Off

With the remote on/off function the system can be switched on and of through an external control signal. When active the internal software goes from the run state into the shutdown state. After a predefined timeout the PCU switches the main power supply off. The timeout can be configured through S14.

Config switch S14 position	$t_{debounce\_on}$ On debouncing (setup)	$t_{debounce\_off}$ Off debouncing (hold)	$t_{startup}$ Hold time until switch off signal is routed to processor, if system is still booting	t_{hard_off} Timeout until switch off signal is generated from processor (after that hard off)
0	-	-	-	-
1	2 s	60 s	5 s	1 min
2	2 s	60 s	60 s	5 min
3	2 s	60 s	30 min	2 h
4	2 s	60 s	2 h	2 h
5 – F	N/a	n/a	n/a	n/a

Tab. 28 PCU timing configuration through S14

When switch S14 is in position 0 the PCU is in bypass mode.

Application example

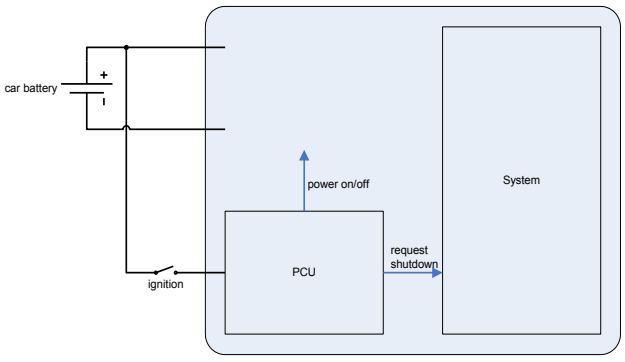

Fig. 7 Application example: CAR PC

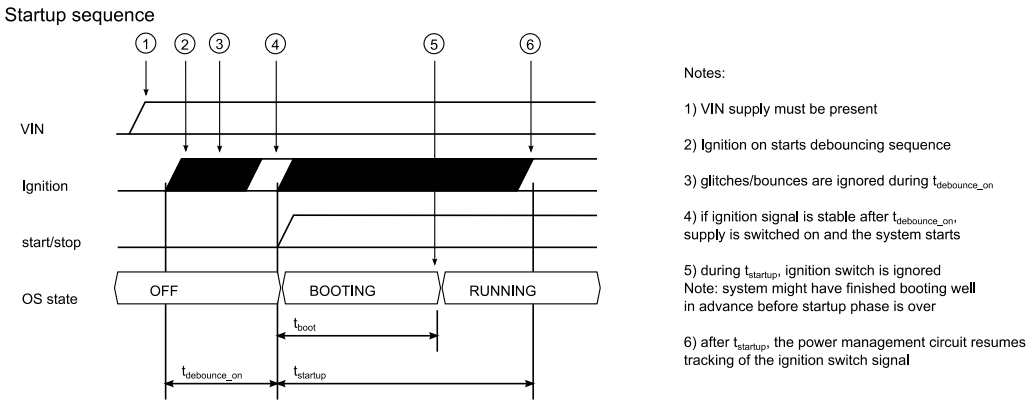

Fig. 8 Startup timing diagram

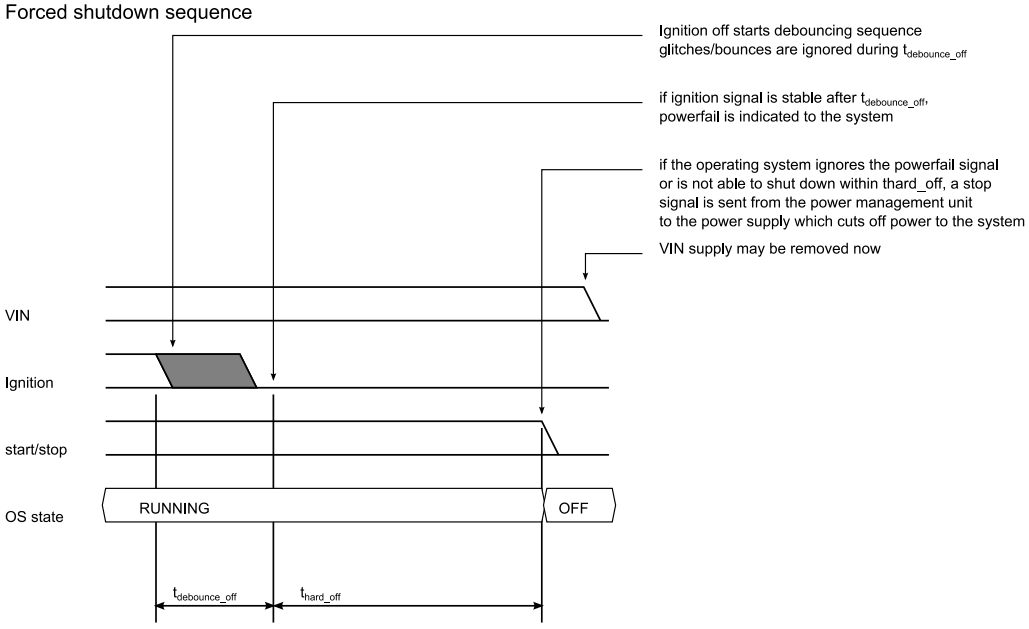

Fig. 9 Shutdown timing diagram

Important Notes

The operating system must support the remote on/off function.

3.3.16. PC/104 Bus Interface

The internal PC/104 bus interface of the M41F08 allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown in Tab. 29. See paragraph 7.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
						A2	⊗	SD7	B2	⊗	RESETDRV
F1	⊗	GND	E1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
F2	⊗	SMB_CLK	E2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
F3	⊗	SMB_DAT	E3	⊗	SMB_ALRT#	A5	⊗	SD4	B5	⊗	-5V (optional)
F4	⊗	Vbatt	E4	⊗	STOP#	A6	⊗	SD3	B6	⊗	DRQ2
F5	⊗	+12V (optional)	E5	⊗	+12V (optional)	A7	⊗	SD2	B7	⊗	-12V (optional)
F6	⊗	GND (optional)	E6	⊗	GND (optional)	A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (optional)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
D20	⊗	reserved	C20	⊗	reserved	A29	⊗	SA2	B29	⊗	+5V
D21	⊗	reserved	C21	⊗	reserved	A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 29 PC/104 Bus Connectors PA/PB, PC/PD

The M41F08 board is not fully IEEE 996.1 (PC/104) compliant. The following restrictions and differences to the IEEE 996.1 specification apply:

- connector is compatible but the monting holes are not
- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)

Important Note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the M41F08 board or add-on boards.

3.3.17. Frontside Status LEDs

The two colored LEDs on the front side show the following states:
Green LED - Board ready (programming see Setup register in chapter 4)
Red LED - STOP signal (programming see Control register in chapter 4)

4 Programming Information

4.1. Overview

The programming of the M41F08 board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS. For detailed information refer to the NETIPC firmware documentation and other related documents as listed in paragraph 1.3. Please contact Syslogic technical support if you need special BIOS configuration.

4.2. Interrupt, Memory and I/O Resources

4.2.1. Interrupt Resources

The following table shows the usage of the M41F08 interrupt inputs. Interrupts marked 'shared' are shared between an onboard device and an PC/104 bus interrupt line. These interrupts should only be used for multiple interrupt sources, if all interrupt routines are able to process shared interrupts (normally not the case for keyboard, COM1/2, Ethernet, Mouse and IDE interrupt drivers). Interrupts marked 'free' are not used by onboard devices if they are not assigned to a PCI device in the BIOS configuration.

Interrupt	Interrupt Source	Remarks
Master		
IRQ0	Timer Channel 0	
IRQ1	PS/2-Controller (Keyboard)	
IRQ2	Slave Interrupt Controller Cascading	
IRQ3	COM2	
IRQ4	COM1	
IRQ5	COM4	
IRQ6	PC/104 Bus IRQ6	free
IRQ7	LPT1	
Slave		
IRQ8	Real Time Clock	
IRQ9	ACPI/PCI	do not connect
IRQ10	COM3	
IRQ11	CAN1, CAN2	
IRQ12	PS/2-Controller	
IRQ13	Floating Point Unit	
IRQ14	Primary IDE Channel	do not connect
IRQ15	PC/104 Bus IRQ15	free
Special		
NMI	Watchdog and PC/104 Bus Error Interrupt IOCHCK*	shared

Tab. 30 Interrupt Usage

4.2.2. Memory Resources

The general memory layout is shown in paragraph 3.2.1. The configuration of the memory layout is done by programming processors internal configuration registers and board configuration registers (see paragraph 4.2.3). This is done completely by the BIOS on system startup and must not be changed during operation. For operating systems requiring memory configuration (e.g. Windows CE) the memory layout shown in paragraph 3.2.1 must be considered.

4.2.3. I/O Resources

This paragraph describes only the M41F08 system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 3.2.2. Peripheral devices are discussed in paragraph 0. Note that the Socket Memory related registers are programmed by the BIOS on system startup and must not be changed during operation except for the Socket Memory Window Mapping Register in case of user controlled memory mapping (allowing access to 512kbyte Socket Memory as eight 64kbyte blocks in the Socket Memory window below 1M in Real Mode).

Address	Device / Register	Remarks
8200H	Status Register	
8201H	Control Register	Reset state = 05H
8202H	Function ID Register	
8203H	reserved	do not write
8204H	Option ID Register	
8205H	Setup Register	Reset state = 00H
8206H	Revision ID Register	
8207H	Socket Memory Configuration Register	Reset state = 00H
8208H	Socket Memory Window Mapping Register	Reset state = 00H
8209H	Socket Memory Window Base Address Register	Reset state = D0H
820AH	Boot Mode Input Register	
820BH	I2C Register for Temp Sensor	
820CH	reserved	
820DH	PWM-Register for LCD Inverter Brightness Control	Reset state = 00H
820E..821FH	reserved	do not access

Tab. 31 M41F08 System Registers

Status Register 8200h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OVRTMP#	LOBAT#	1	WDG#	ERRFLG#	ATTFLG#	ERRINT#	ATTINT#	Read
reserved								Write
1111'1111 (0xFF)								Reset

Description:

OVRTMP# Temperature Sensor Status Flag

Read	Write
0 = programmed temp. limit reached 1 = temperature ok (below limit)	

LOBAT# Battery Status Flag

Read	Write
0 = Battery voltage low 1 = Battery voltage ok	

WDG# Watchdog Status Flag

Read	Write
0 = Watchdog has timed out 1 = Watchdog running or disabled Reset by issuing a hardware reset (see register 8204hex)	

ERRFLG# Error Status Flag (for polled applications)

Read	Write
not used, returns 1	

ATTFLG# Attention Status Flag (for polled applications)

Read	Write
not used, returns 1	

ERRINT# Error Interrupt Status

Read	Write
0 = Error Interrupt pending 1 = No error interrupt pending	

ATTINT# Attention Interrupt Status Flag

Read	Write
not used, returns 1	

Reserved Reserved, always write 0

Control Register 8201h

D7	D6	D5	D4	D3	D2	D1	D0	Access
TRIG#	WDTRIG	WDNMI	STOP	TRGSRC	FREEZE	ERREN#	ATTEN#	Read
TRIG#	WDTRIG	WDNMI	STOP	TRGSRC	FREEZE	ERREN#	ATTEN#	Write
0000'0101 (05h)								Reset

Description:

TRIG# Bus Trigger (currently not supported)

Read	Write
readback of written value	

WDTRIG Watchdog Trigger

Read	Write
readback of written value	Any state change triggers the watchdog.

WDNMI Watchdog NMI Configuration

Read	Write
0 = Watchdog activates hardware reset 1 = Watchdog timeout activates Non Maskable Interrupt (NMI)	0 = Watchdog activates hardware reset 1 = Watchdog timeout activates Non Maskable Interrupt (NMI)

STOP NETSBC Stop# Signal State

Read	Write
0 = STOP# inactive (high), red LED off 1 = STOP# active (low), red LED on	0 = STOP# inactive (high), red LED off 1 = STOP# active (low), red LED on

TRGSRC Trigger source selection

Read	Write
not used, returns 0	

FREEZE Freeze bit

Read	Write
not used, returns 1	

ERREN# Error Interrupt Enable (PC/104 bus IOCHCK# routed to NMI)

Read	Write
always 0 = Error Interrupt on NMI	

always enabled	

ATTEN# Attention Interrupt Enable

Read	Write
not used, returns 1	

The STOP# signal is intended for control of add-on boards. It is available on the PC/104 bus connector extension PE.

STOP# is intended as signal to force an add-on board function to a specified state. For example with the digital I/O board IPC/DIO32 the STOP# signal is used to either reset or freeze the state of the digital outputs depending on setup of the DIO32 board as long as the STOP# signal is active (low).
The STOP# signal also directly drives the red LED on the front (STOP# low = LED on).
Upon startup STOP# is active (LED on) until the BIOS has initialized the main peripherals, it is set inactive (LED off) before booting the operating system. STOP# is also active (LED on) while operating in Bootloader mode.

Function ID Register 8202h

D7	D6	D5	D4	D3	D2	D1	D0	Access
FID[7:0] Function ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

FID Function ID

Read	Write
51h = general IPC processor board	reserved, always write 0

Option ID Register 8204h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OID[7:0] Option ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

OID Option ID

Read	Write
E0h = M41F08/S41F08	A5h = Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit) 5Ah = Writing data 5Ah invokes a complete power off or power reset (also clearing the Watchdog timeout status bit), system restarts depending on configuration of power management controller.

Setup Register 8205h

D7	D6	D5	D4	D3	D2	D1	D0	Access
READY	WDEN	0	0	0	0	0	USBEN	Read
READY	WDEN	0	0	0	0	0	USBEN	Write
0000'0001 (01h)								Reset

Description:

READY Ready bit, green LED

Read	**Write**
0 = Inactive, green LED off 1 = Active, green LED on	0 = Deactivate green LED 1 = Activate green LED

WDEN Watchdog enable

Read	**Write**
0 = Watchdog disabled 1 = Watchdog enabled (running)	0 = Disable watchdog 1 = Enable watchdog

USBEN USB Power enable

Read	**Write**
0 = USB power off 1 = USB power on	0 = disable USB power 1 = enable USB power

The READY signal directly drives the green LED on the front (READY high = LED on).
Upon startup READY is inactive (LED off) until the BIOS has initialized the main peripherals, it is set active (LED on) before booting the operating system.
Always read back the current state before programming this setup register for enabling the watchdog!

Important Note

Be careful when disabling USB power by setting USBEN=0 since this also disables any USB HID (keyboard, touch). Always use a program sequence which automatically reenables USB power some seconds later. The PS/2 keyboard port is not affected by this.

Revision ID Register 8206h

D7	D6	D5	D4	D3	D2	D1	D0	Access
RID[7:0] Revision ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

RID Logic Design Revision ID

Read	Write
see Product Revision History	

reserved Reserved, always write 0

Socket Memory Configuration Register 8207h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved reserved

Read	Write
0	

Reserved reserved, do not write

Socket Memory Window Mapping Register 8208h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved reserved

Read	Write
0	

Reserved reserved, do not write

Socket Memory Window Base Address Register 8209h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	0	0	Read
reserved								Write
0000'0000 (0x00)								Reset

Description:

Reserved reserved

Read	Write
0	

Reserved reserved, do not write

Status Register 820Ah

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	0	0	BM1	BM0	Read
reserved								Write
0000'0011 (0x03)								Reset

Description:

BM1..0 Boot Mode Inputs

Read	**Write**
0 = reserved 1 = reserved 2 = reserved 3 = normal Operating Mode	

Reserved reserved, do not write

I2C Register 820Bh for temperature sensor control

D7	D6	D5	D4	D3	D2	D1	D0	Access
SCLO	SDAO	SCL	SDA	1	1	1	1	Read
SCLO	SDAO	Reserved, always write 1						Write
FFh								Reset

Description:

SCLO Clock Port Output State

Read	Write
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SDAO Data Port Output Port Latch State

Read	Write
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SCL Clock Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

SDA Data Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

PWM Register 820Dh for LCD Inverter Brightness Control

D7	D6	D5	D4	D3	D2	D1	D0	Access
PWM preset D[7..0]								Read
PWM preset D[7..0]								Write
80h								Reset

Description:

D[7..0] PWM Preset Register

Read	**Write**
D[7..0] = Preset Value	D[7..0] = Preset Value

The PWM value, may be translated to a voltage depending on setting of configuration switch S5. Value 0 corresponds to voltage level 0, value FFh corresponds to maximum voltage level (2.5V or 5V). Please check inverter datasheet for translation of voltage level to brightness.

4.3. Peripheral Devices

4.3.1. VGA/LCD-Interface

The VGA interface uses the standard PC/AT VGA register set. For detailed programming information please refer to the IBM PC/AT Technical Reference or similar documentation.
Low level programming is handled by the VESA compatible VGA-BIOS.
For custom LCD BIOS requirements please contact Syslogic technical support.

4.3.2. IDE-Interface

The IDE interface uses the standard PC/AT register set. For detailed programming information please refer to the IBM PC/AT Technical Reference, ATA/ATAPI standards (ANSI) or similar documentation.

4.3.3. Serial Ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit fifos. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation.

4.3.4. Keyboard Interface

The Keyboard interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 8042 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.5. Ethernet Interface

On the M41F08 board the Ethernet interface LAN1 uses the RDC R6040 Ethernet Controller. For detailed programming information and drivers check www.syslogic.com and www.dmp.com.tw.
The Ethernet interface LAN2 uses the intel 82574IT Ethernet Controller. For detailed programming information and drivers check www.intel.com .

4.3.6. USB Interface

The USB interfaces use the standard OHCI/EHCI register set. Legacy support and low level programming is handled by the BIOS and standard OS drivers.

4.3.7. Temperature Sensor

The Temperature Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the M41F08. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.
Poweron default setting for OVERTMP* is 80°C chip temperature.

4.3.8. Watchdog

The watchdog is disabled by default on poweron and must be enabled either by the BIOS or by the application program.
If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the M41F08 Setup Register, the watchdog action (RESET or NMI) must be programmed in the M41F08 Control Register (bit WDNMI).
If RESET activation is selected, the watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the M41F08 Control Register. The application must check the WDG* bit in the M41F08 Status Register uppon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the M41F08 Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.
If NMI activation is selected, the watchdog generates a Non Maskable Interrupt to the processor if it is not triggered within the configured timeout window by writing the WDTRIG bit in the M41F08 Control Register. Note that enabling the NMI input of the processor also requires setting bit 7 of I/O port 70h (NMI mask) and clearing bit 3 of I/O port 61h (Port B IOCHK# enable). The NMI routine must check the WDG* bit in the M41F08 Status Register to identify the watchdog as the source of the NMI, and it must issue a hardware reset (by writing the value 0a5h to the M41F08 Option ID Register) to clear the WDG* flag. Otherwise the NMI routine is entered again as soon as the watchdog is started.
Sample code showing the initialisation and triggering of the watchdog is available for RESET and NMI mode in the free IPC/IOCOMSW-1A package.

Note

The NMI mask bit (bit 7 of I/O port 70h) is write only. Typically it is enabled by the BIOS and should not be disabled by application software.

4.3.9. PC/104 Bus Interface

For detailed description of PC/104 add-on board programming please consult PC/104 and ISA bus standard documentation and related PC/AT architecture literature as well as the add-on boards documentation.

5 Installation and cabling

5.1. Introduction

Installation and cabling of the IPC/ M41F08 system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail or mounting kit.

Important note

Before applying power to the M41F08 system, the main board must be configured correctly.

Important notes

To meet the requirements of EMI/RFI "CE"-certification, correct mounting, installation and cabling of the M41F08 system according to these guidelines is absolutely necessary.

5.2. Powering the M41F08 System

The "logic supply voltage", i.e. the power driving the electronic circuits (CPU and base board) is internally generated from the 12/24VDC power supply input. Remember that the power supply is non-isolated. For an isolated version please contact the manufacturer.
The power supply has to be connected according to paragraph 3.3.12. Maximum allowed cable length between ac/dc power supply and system power input is 30 m. If the cable is longer than 30 m or routed outside the building, special overvoltage and filtering elements have to be installed to comply with the requirements of EMI/RFI "CE"-certification.

When selecting the external power supply the maximum power dissipation of the system has to be considered.

Important botes

Please make sure that the input voltage does not exceed the recommended operating range otherwise the electronics board could get damaged and correct operation cannot be guaranteed.
Use an overload protected power supply to prevent damage in case of a short inside the system.
The ac/dc power supply must fulfill the requirements for EMI/RFI "CE"-certification.

5.3. Cabling the interfaces

Use appropriate cabling for all interfaces. Shielded cabling is required to meet the EMI/EMC limits.

5.4. Grounding

In some cases it is recommended to connect the shields of the cables to chassis potential at the entry point into the housing cabinet as shown in Fig. 10. If the cables enter a hermetically closed cabinet, use special 360 degree metal clamps (EMI/RFI protected types which contact to the cable shield).

Important notes

Grounding of the cables shields using "pig-tail wires" are not recommended because of their high impedance at high frequencies. It is better to clamp the shields onto a grounded copper rail.

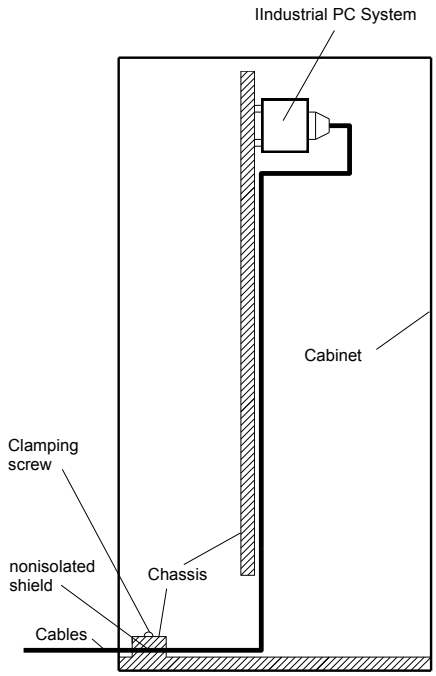

Fig. 10 Additional grounding of the cable shields at the entry point of a cabinet.

5.5. Cabling of communication links

If the communication ports are unisolated ports, cable shields have to be connected to chassis potential on both sides of the interconnection cable. If the cable is very long, a thick copper wire (10 mm^2) for potential adjustment is highly recommended. Fig. 11 shows an non isolated system with common chassis ground.
Some of the communication ports are galvanically isolated ports. In such cases the shield of the interconnection cable must be wired to chassis potential only on one side of the cable. Fig. 12 shows an isolated system with independent grounds.

Important notes

Grounding of cable shields using "pig-tails wires" are not recommended because of their high impedance at high frequencies. It is recommended to clamp the shields onto a grounded copper-rail.

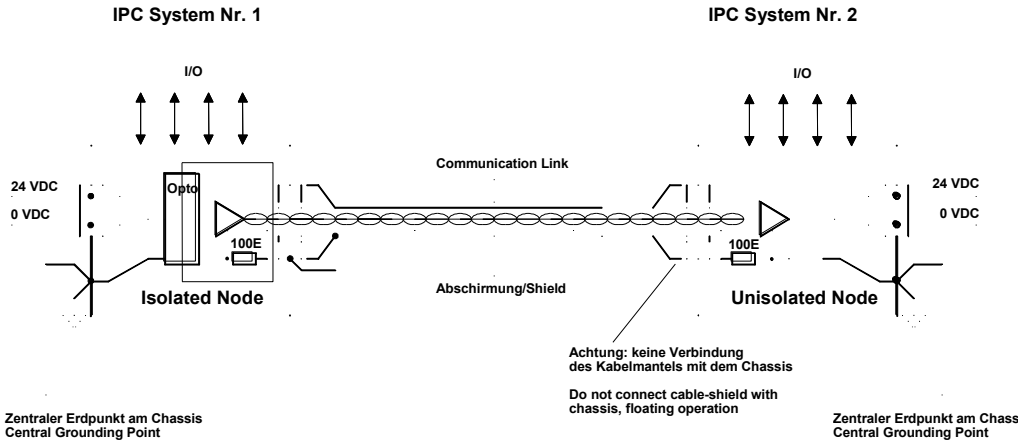

Fig. 11 Non isolated communication link with common chassis potential

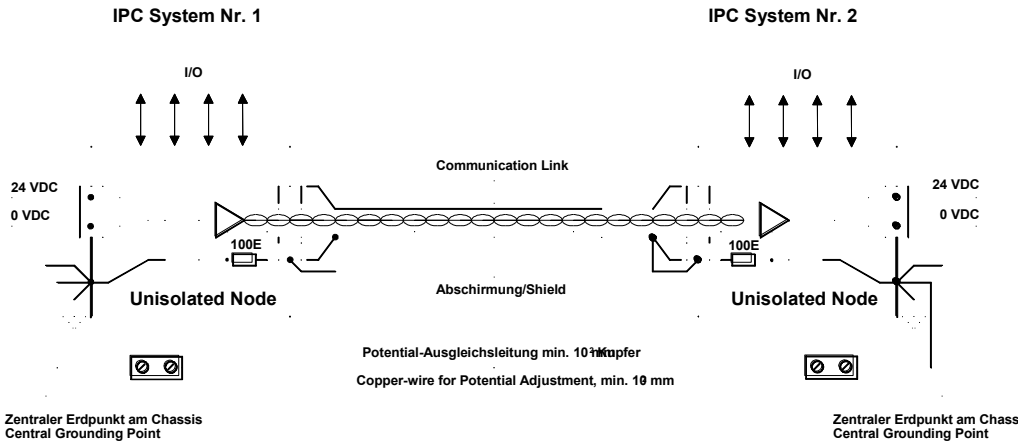

Fig. 12 Isolated communication link

6 Service

6.1. Replaceable Parts

This system contains the following replaceable parts:

- CFast flash card
- Main fuse
- Litium battery (selected product variants only)

To replace the flash card power off the system and remove the service cover. After having unlocked the clip, the flash card may be removed. When inserting a new flash card be sure that it is fully compliant with the CFast standard. Syslogic highly recommends CFast flash cards specified for industrial use by the card manufacturer. Check temperature range and durability to comply with your requirements.

To replace the battery power off the system and remove the service cover. Pull out the batter<y carefully.
Replacement battery must be one of the following types:

- Renata CR2450N (3V, 540mAh)
- Renata CR2477N (3V, 950mAh)

Caution! Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according the manufacturer's instructions.
Because the self-discharge of all Lithium Batteries increases rapidly at high temperatures the battery life time decreases by a great amount. To prevent battery leakage scheduled service/replacement is recommended. Please contact the battery manufacturer for further details and calculation assistance for battery life time calculation.

The main fuse protects the system against destruction in case of high energy distortions on the power line. For replacement, the system must be opened in a ESD protected environment with power removed. Only an entitled instructed person is allowed for this operation. Replacement fuse type is Littlefuse 45203.0L (3A slow-blow).
Safety warnings and installation guidelines must be followed according to paragraphs 1.6, 1.8 and 5.

7 Technical Data

7.1. Electrical Data

Important Note

Do not operate the M41F08 system outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute Maximum Ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
power supply voltage	Vcc	-0.5		30	Vdc
isolation logic to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RJ45 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation CAN to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation CAN to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RS485 to logic (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
isolation RS485 to chassis (AC, 60s, 500m a.s.l., Ta=25°C)		500			Vrms
creepage distances:					
logic to chassis and PCB boarder		1.0			mm
logic to mounting holes		0.5			mm
RJ45, CAN, RS485 to logic		1.0			mm
RJ45, CAN, RS485 to chassis and PCB boarder		1.0			mm
storage temperature range[1]	Tst	-40		90	°C

Tab. 32 General Absolute Maximum Ratings

[1]Due to the large effect of self-discharge at high temperature of the Lithium Battery it is recommended to store the device at around +25°C.

Recommended Operating Conditions

Parameter	Symbol	min	nom	max	
power supply voltage	Vcc	9.0	12/24	30	Vdc
battery backup voltage (Io=100µA)	Vbatt	2.7	3.0	3.3	Vdc
PS/2 connector (P3/P4) power load (+5V)	Ips2			200	mA
operating free-air temperature range (standard products)	Ta	-40		70	°C

Tab. 33 General Recommended Operating Conditions

Electrical Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	typ	max	Unit
power supply current (Vcc=24V, no external loads)	Icc		0.35		A
power supply current (Vcc=12V, no external loads)	Icc		0.7		A
full load power dissipation (worst case, no external loads)	Pmax		10	14	W
GoldCap RTC buffer time (Vcc=off)			>24		h
Vbatt loading (Vcc=off)	Ibat(off)		10	30	uA
Vbatt loading (Vcc=on)	Ibat(on)		5	10	uA
LOWBAT* trip point		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			1.3		V
LCD inverter enable control disable state	Il<4mA	0		0.4	V
LCD inverter enable control enable state	Ih<4mA	2.4		5	V
LCD inverter brightness control	I=10mA	0		5	V

Tab. 34 General Electrical Characteristics

Switching Characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
processor clock	fcpu		800		MHz
UART base clock	fuart		1.8459		MHz
COM1/2/3/4 baud rate				115.2	kbaud
Watchdog timeout (short period)	Tw	70	100	140	ms
Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock	ftimer		1.19318		MHz
Timer base clock accuracy				+/-100	ppm
Timer base clock aging				+/-5	ppm/year
Real Time Clock base clock	frtc		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year
LCD inverter brightness PWM base clock	fpwm		16		kHz

Tab. 35 General Switching Characteristics

7.2. EMI/EMC Data

The M41F08 system fulfills the following standards:
Emission: EN55022 / CISPR 22 Class A and EN50121-3-2
Immunity: EN55024 / CISPR 24 and EN50121-3-2

Important Note
The M41F08 system is a class A system for industrial applications. It is not indented for use in residential or home applications.

7.3. Mechanical Data

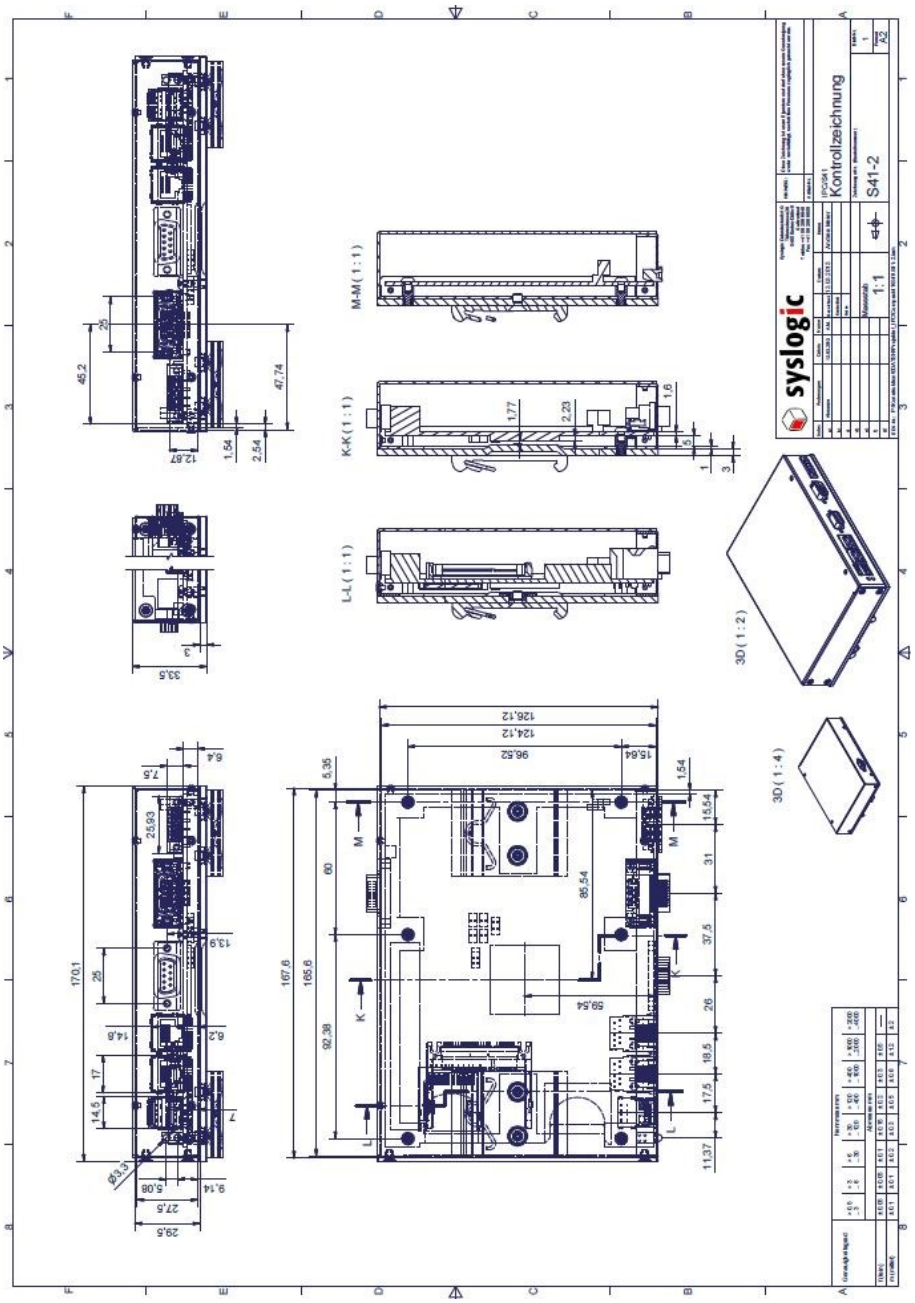

Fig. 13 Mechanical Outline Enclosure S

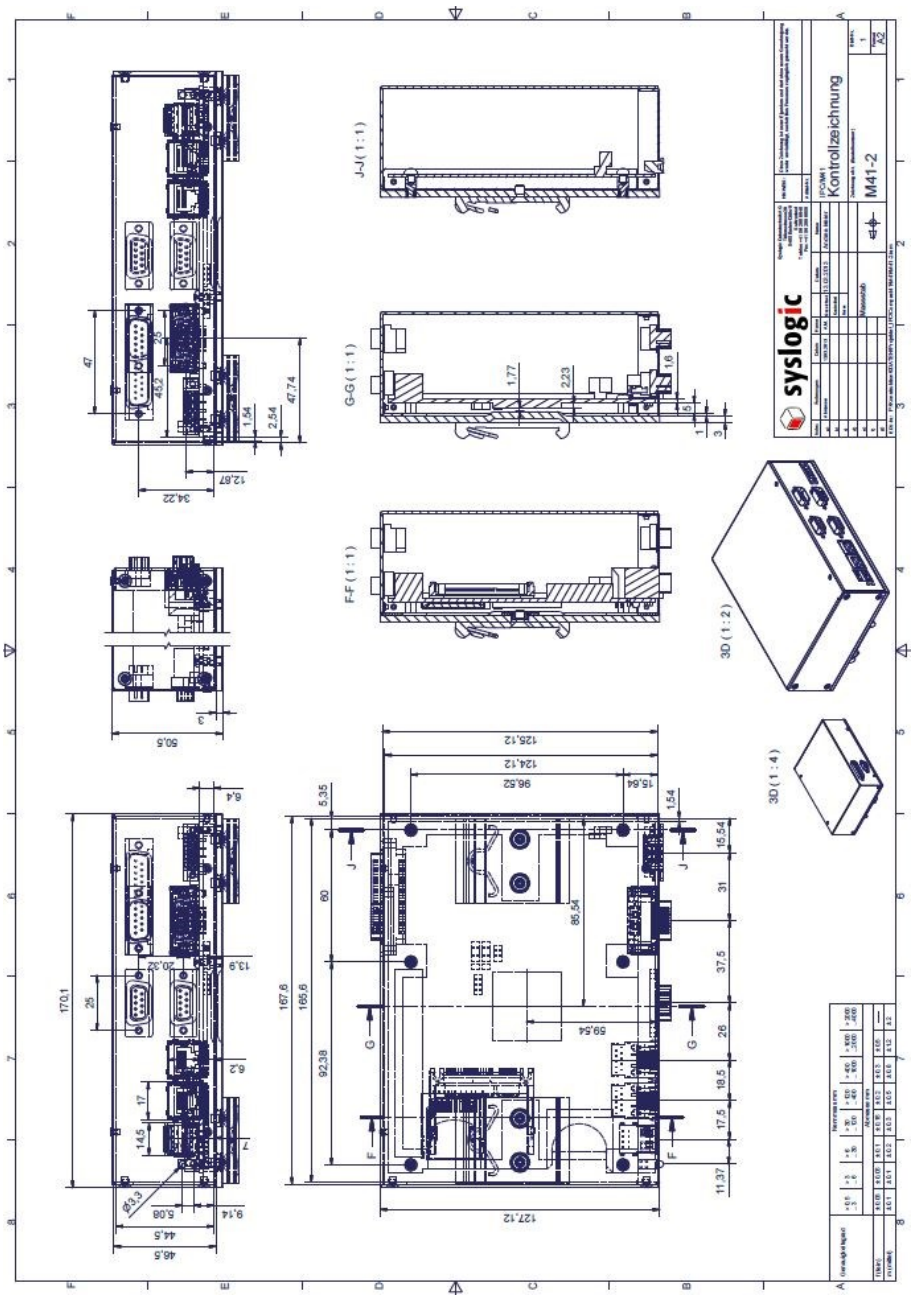

Fig. 14 Mechanical Outline Enclosure M

8 Firmware

8.1. Software Structure

The x86 CPU board based PC/104 system is based on the following software structure:

BIOS (Basic Input/Output System)

- Power On Self Test (POST)
- Initialization of standard peripheral devices
- Boot procedure for the Operating System

  Note : Refer to the BIOS documentation for detailed information

OS (Operating System)

- Initialization of additional peripheral devices
- Start procedure for the Application Programs

  Note : Refer to the OS documentation for detailed information

Application Programs

- Initialization of M41F08 system, communications and external devices
- Start procedure for the Control Tasks

  Note : Refer to the Application Programs documentation for detailed information

8.2. Firmware Functions

The M41F08 board is setup with BIOS firmware. Some standard PC/AT peripheral devices (e.g. VGA, Keyboard/Mouse, Serial Ports, IDE interface) are directly supported by the BIOS, BIOS extensions and Operating Systems. Some peripheral devices (e.g. Ethernet) are directly supported by standard communication software (e.g. TCP/IP stacks, TCP packet drivers) others need special programming according to the freely available sample software IPC/IOCOMSW-1A (e.g. Watchdog). Please refer to the appropriate documentation for detailed information.

8.3. Application Programming Interface (API)

The M41F08 system does not contain any special API beside the installed BIOS. Refer to the BIOS and Operating System documentation for API specifications.

9 Product Revision History

9.1. Hardware

This paragraph lists the different hardware revisions of the M41F08 systems delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Revision ID Register	Remarks
IPC/ M41F08-AxxxE #1	1	01H	Original Release
IPC/ S41F08-AxxxE #1	1	01H	Original Release

Tab. 36 Hardware Revision State

9.2. Hardware Erratas

This paragraph lists some important erratas of the current M41F08 boards to enable workarounds in user software. Additional erratas might be present but a workaround already implemented in the BIOS. It is important therefore that neither the application software nor the operating systems reprograms the processor chipset's configuration registers.
Note that prototype board erratas (boards with revision #0) are not listed here. Contact Syslogic technical support for prototype board information.

9.3. Firmware

There is currently no errata information available.

Important Note

This document always covers the latest product revision listed in .
Please contact the manufacturers technical support for upgrade options.

10 Manufacturer Information

10.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG, Switzerland
Web: http://www.syslogic.com
Email: info@syslogic.com
Technical support: support@syslogic.com

10.2. Warranty

Our products are covered by a world-wide manufacturer's warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a job number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.