IPC/ML71xxx-xxxE

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0.2	15.02.2013	F. Liechti	Reworked Power Fail
1.0	16.05.2013	R. Newbould	Release Version
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1.3	06.09.2014	F. Liechti	Power management description modified

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1 Introduction

1.1. General remarks

The content and presentation of this document has been carefully checked. No responsibility is accepted for any errors or omissions in the documentation.

Note that the documentation for the products is constantly revised and improved. The right to change this documentation at any time without notice is therefore reserved.

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CompactFlash	trademark of SanDisk Corporation
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PCI/104	trademark of PC/104 Consortium
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1.2. Contents of this documentation

This document addresses to system integrators, programmers and instructed installation and maintenance personal working with the system. It provides all information needed to configure, setup and program the IPC/ML71xxx-xxxE systems.

1.3. Naming conventions

Throughout this documentation the product is referenced through it's marketing name "IPC/ML71".

The same applies to the integrated base board. Throughout this documentation it will be referenced as "IPC/BL71".

1.4. Additional products and documents

1.4.1. Software products

There are no additional software products except operating systems:

- Operating Systems: check chapter 6.4 for a list of supported implementations.

1.5. Documents and references

1.5.1. Syslogic documentation

- CPU module documentation: DOC/ATOME6-E (cem_atome6_e.pdf)

1.5.2. Standards and books

The following documents are *useful* for additional information about PC/104 and IEEE 996.1:

- PC/104 Specification Version 2.3
- PCI/104 Specification Version 1.0

- IEEE 996: IEEE standard document 'Personal Computer Bus Standard'
- IEEE 996.1: IEEE standard document 'Compact Embedded-PC Modules'

The PC/104 Specification may be downloaded from the Internet (see address below).

- PC/104 Consortium
  www.pc104.org

The IEEE standard documents may be ordered directly from the IEEE or any standards document distributor (see addresses below).

- IEEE Standards Department
  www.ieee.org

- 'ISA & EISA, Theory and Operation' by Edward Solari (Annabooks, San Diego), ISBN 0-929392-15-9
- 'PCI System Architecture' by Tom Shanley / Don Anderson (Mindshare, Inc.), ISBN 0-201-30974-2

1.5.3. Datasheets

For additional and more detailed information on the Intel Atom processor and chipset the following documents are of interest:

- Datasheet Intel Atom Processor E6xx Series
  http://download.intel.com/embedded/processor/datasheet/324208.pdf#iid=3790

- Specification Update Intel Atom Processor E6xx Series
  http://download.intel.com/embedded/processor/specupdate/324209.pdf?iid=3876#iid=3876

- Datasheet Intel Platform Controller Hub EG20T(PCH)
  http://download.intel.com/embedded/chipsets/datasheet/324211.pdf#iid=3791

- Specification Update Intel Platform Controller Hub EG20T (PCH)
  http://download.intel.com/embedded/processor/specupdate/324209.pdf?iid=3876#iid=3876

- Datasheet Intel 82574 GbE Controller Family
  http://download.intel.com/design/network/datashts/82574.pdf

- Datasheet NXP SJA1000
  http://www.nxp.com/documents/data_sheet/SJA1000.pdf

- Application Note AN97076: SJA1000 – Stand-alone CAN controller
  http://www.nxp.com/documents/application_note/AN97076.pdf

1.6. Items delivered

- Will be inserted in a future release of this document.

1.7. Safety recommendations and warnings

The products are intended for measurement, control and communications applications in industrial environments. The products must be assembled and installed by specially trained people. The strict observation of the assembly and installation guidelines is mandatory.
The use of the products in systems in which life or health of persons is directly dependent (e.g. life support systems, patient monitoring systems, etc.) is not allowed.

The use of the products in potentially explosive atmospheres requires additional external protection circuitry which is not provided with the products.
In case of uncertainty or of believed errors in the documentation please immediately contact the manufacturer (address see chapter 11). Do not use or install the products if you are in doubt. In any case of misuse of the products, the user is solely liable for the consequences.

Important note
Ensure that the power supply is disconnected from the device before working on the device (connecting interfaces, replacing flash cards, batteries, opening the enclosure, etc.).

Important note
Please read the safety instructions of the power supply before installing/connecting the device.

1.7.1. EMC

Important note
This is a Class A product and not intended to be used in domestic environments. The product may cause electromagnetic interference. Appropriate measures must be taken.

1.7.1. Battery

Important note
Caution! Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

1.7.2. Hot surface

Important note
Do not touch the surface of the device during operation. It may be hot and cause burns.

1.8. Electro-static discharge

Electronic boards are sensitive to Electro-Static Discharge (ESD). Please ensure that the product is handled with care and only in an ESD protected environment. Otherwise a proper operation is not guaranteed and the warranty is not applicable.

1.9. Life cycle information

1.9.1. Transportation and storage

During transportation and storage the products must be in their original packing. The original packing contains a box with antistatic and shock-absorbing material. It is recommended, to keep the original packing in case of return of the product to the factory for repair. Note that the packing is recyclable.

1.9.2. Operation

The operating environment must guarantee the environmental parameters (temperature, power supply, etc.) specified in the technical specification section of the product manuals.
The main functionality of the IPC system is defined by the application programs running on the processor board. The operating system and application programs are not part of the delivery by Syslogic but are defined, developed and tested by the customer or a system-integrator for each specific application. Refer to the respective documentation for more information.

1.9.3. Maintenance and repair

The IPC system features error- and malfunction-detection circuitry. Diagnostic information gathered is transferred to the applications software where it can be used. In the rare case of a module hardware-failure or malfunction, the complete board should be exchanged. The faulty board must be returned to the factory for repair. Please use whenever possible the original packing for return of the product (ESD and mechanical protection).

1.9.4. Warranty

Our products are covered by a world-wide manufacturer's warranty. The warranty period starts at the delivery time from our official distributor to the customer. The duration of the warranty period is specified in the respective product catalogs and the offers. All products carry a serial number for identification. The manufacturing data and deliveries are registered in a high level Quality Management System.
The warranty covers material and manufacturing defects. All products must be returned via the official distributor to the factory for repair or replacement. The warranty expires immediately if the products are damaged of operation outside of the specified recommended operating conditions. The warranty also expires if the date code or job number listed on the product is altered or rendered unintelligible. The warranty does not include damage due to errors in firmware or software delivered with the products.

1.9.5. RoHS

The products of the IPC/ML71 family are designed and produced according to the Restriction of Hazardous Substances (RoHS) Directive (2011/65/EC).

1.9.6. Disposal and WEEE

At the end of the life span the IPC products must be properly disposed. IPC products contain a multitude of elements and must be disposed like computer parts. Some of the IPC products contain batteries which should be properly disposed.
The products of the IPC/ML71 are not designed ready for operation for the end-user and intended for consumer applications. Therefore the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) is not applicable. But users should still dispose the product properly at the end of life.

2 Product description

2.1. IPC/ML71 Systems

The IPC/ML71 contains an enclosure and the IPC/BL71 motherboard. A list of main features can be found in the table below:

2.2. Features

2.2.1. CPU core

- Intel Atom E680T (Tunnelcreek) single core processor for mobile devices
- industrial temperature range (-40..+85C)
- IA32 processor based on Intel's 45nm Hi-k metal gate silicon technology
- Multiple micro-ops per instruction are combined into one micro-op and executed in a single cycle
- in-order execution core
- high performance 32-bit 16-stage pipeline
- energy efficient branch prediction
- 1.6GHz processor clock
- 32kB, 4-way instruction and 24kB, 6-way data L1 cache with parity
- 512kB, 8-way L2 cache with ECC
- 32-bit wide DDR SDRAM interface
- supports Intel Hyper Threading Technology (HTT), 2 threads
- supports Intel Virtualization Technology (VT-x)
- supports Enhanced Intel Speedstep Technology
- PCIe as front side bus, 2.5GB/s, 1.0a Base Specification compliant (4 x1 lanes)

2.2.2. Memory

- up to 2048 Mbyte DDR2 SDRAM on board (device width x16)
- 800MT/s data rate
- 32bit data width

2.2.3. Graphics controller

- integrated Intel Graphics Media Accelerator 600 (Intel GMA600)
- power optimized 2D/3D graphics engine (max. 400MHz)
- integrated graphics device (IGD) includes LVDS and SDVO display ports
- LVDS max pixel clock 79.5MHz (equates to 1280x768 @ 85Hz)
- SDVO max. pixel clock 160MHz (equates to 1280x1024 @ 85Hz)
- Supports Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3)
- Supports full hardware acceleration for H.264, MPEG2, MPEG4, VC1 and WMV9
- high performance 2D 64-bit graphics controller with backwards compatibility to VGA and SVGA standards

2.2.4. CFast and SATA interface

- CFast connector for onboard mountable CFast card
- standard SATA connector

2.2.5. Integrated peripherals

- integrated peripheral controller (IPC) with PC/AT compatible DMA controllers (2 x 8237), interrupt controllers (2 x 8259) and timer/counter channels (8254)
- hardware watchdog configurable for 100 ms or 1.6 s timeout, hardware reset activation
- temperature supervisor for software controlled power management

2.2.6. PS/2 mouse and keyboard interface

- PC/AT compatible keyboard controller (8242 compatible) with PS/2 mouse support
- only available on an internal header

2.2.7. Serial ports

- six serial RS232 ports (COM1 – COM6) with 16 byte receive and transmit FIFO (16550)
- optionally COM4 as a non-isolated, half-duplex RS485 interface
- optionally COM5 as an isolated, half-/full-duplex RS485 interface
- optionally COM6 as an isolated, half-/full-duplex RS485 interface

2.2.8. Universal serial bus

- four USB V2.0 ports (OHCI/EHCI-Host Controller) on a standard USB connector
- two USB V2.0 ports (OHCI/EHCI-Host Controller) on internal header

2.2.9. Ethernet

- Up to three 10/100/1000 baseT Ethernet interfaces

2.2.10. Firmware flash memory

- 8 MBit BootBlock Flash for BIOS and setup data (excluding date and time)

2.2.11. Real time clock

- year 2000 compliant Real Time Clock (PC/AT compatible)
- battery backed through onboard battery or header

2.2.12. Configuration switches

- rotary hex switch for customer application

2.2.13. SPI

- SPI interface on internal header
- up to 8MB flash size allowed

2.2.14. SMBus (I2C)

- SMBus v1.0 compliant (3.3V CMOS)
- SMBus interface on internal header

2.2.15. HDA/SPKR

- HDA/SPKR interface on internal header

2.2.16. LPC

- LPC 1.1 compliant interface
- LPC interface on internal header

2.2.17. Power Supply

- onboard non-isolated power supply with wide input range (10Vdc … 30Vdc)
- configurable power supply supervision (this function is only available on systems with revision 2 or higher)
- monitors either external power supply voltage or it can be used as external power fail or on/off input (this function is only available on systems with revision 2 or higher)
- optional isolated power supply

2.2.18. PC/104 Bus Interface

- Subset of standard PC/104 bus interface
- DIN41612 bus connector

2.2.19. CAN Interface

- Two SJA1000 stand-alone CAN controller from NXP (Philips Semiconductor)
- BasicCAN or PeliCAN mode
- supports CAN 2.0A protocol in BasicCAN mode
- supports CAN 2.0B protocol in BasicCAN mode (29 bit identifier accepted)
- sully supports CAN 2.0B protocol in PeliCAN mode
- 16MHz clock frequency
- fixed I/O base addresses
- uses IRQ15
- ISO 11898-24V compatible interface
- optical isolation (1000VDC)
- configurable termination resistor
- standard CAN-OUT DSUB9 connector
- optionally CAN-IN DSUB9 connector

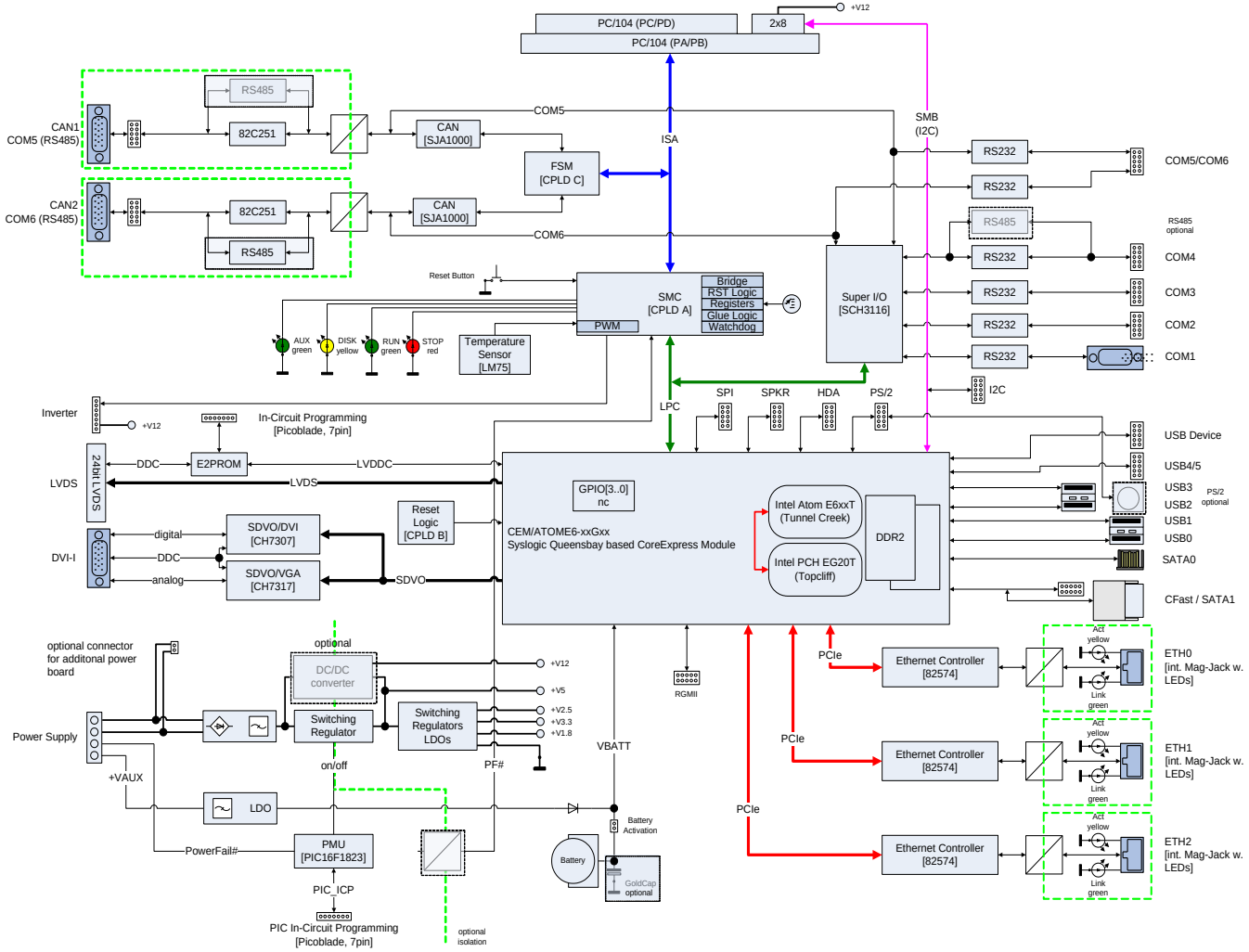


Fig. 1 Block diagram (IPC/ML71)

2.3. Product Variants

Gerät Function Board	IPC/ML71F16-A101E IPC/BL71-101E	IPC/ML71F16-A102E IPC/BL71-102E	IPC/BL71-103E	IPC/BL71-104E	IPC/BL71-105E	IPC/BL71-107E	IPC/BL71-109E
ETH1	X	X	X	X	X	X	X
ETH2	X	X	X	X	X	X	X
ETH3	X					X	
RGMII							
COM1	X	X	X	X	X	X	X
COM2	X	X	(X)	(X)	(X)	(X)	(X)
COM3	X	X			(X)		(X)
COM4	(X)	X	(X) RS485		(X)		(X)
COM5	(X)	(X)					(X)
COM6	X	(X)	(X) RS485				(X)
CAN1	X	X	X				
CAN2		X					
USB0/1	X	X	X	X	X	X	X
USB2/3	X	X	X	X	X	X	X
USB4/5	(X)	(X)	(X)	(X)	(X)	(X)	
USB Device							
DVI	X	X	X		X	X	X
VGA							
LVDS	(X)		(X)	(X)			
Inverter			(X)	(X)			
CFast	X	X	X	X	X	X	X
SATA	(X)	(X)	(X)	(X)	(X)	(X)	
SPI	(X)		(X)	(X)	(X)	(X)	
I2C	(X)		(X)	(X)	(X)	(X)	
HDA/SPKR	(X)		(X)	(X)	(X)	(X)	
LPC	(X)		(X)			(X)	
ISA Bus	(X)						
Reset Button	X	X	X	X	X	X	X
Rotary Switch	X	X	X	X	X	X	X
Temp. sensor	X	X	X	X	X	X	X
Watchdog	X	X	X	X	X	X	X
PM Controller	X	X	X	X	X	X	X
Battery/GoldCap	BAT	BAT	BAT	BAT	BAT	CAP	BAT
CPU	E680T/EG20T 1.6GHz/1GB	E680T/EG20T 1.6GHz/1GB	n/a	n/a	n/a	n/a	n/a

Tab. 1 Feature List

(X) means that the interface is only available on an internal header. Please refer to the following chapter for a more detailed description of the interface and its connector.

3 Hardware description

3.1. Overview

The IPC/IPC/BL71 board hardware may be configured by software (BIOS) and by jumper setting. Software configuration should always be done by using the BIOS Setup. The BIOS Setup can be entered by pressing <F2> at power-up.
The jumper and connector locations are shown in the board layout drawing (Fig. 3).

Important Note

Always check the jumper configuration of a freshly received board to comply with your system requirements before applying power, otherwise the system may get damaged or may fail to operate.

Fig. 2 Board layout (IPC/BL71)

Connector /Header ID	Type	Comment
P1	1x4pin, Rm3.81, 90 Weidmüller SC-SMT 3.81/04/90 LF RL (186398000)	Power Supply
P2	220pin SMX Tyco 3-1827253-6	CoreExpress Bottom side
P3	2x10pin, Rm1.25 Hirose DF13A-20DP-1.25V	LVDS
P4	2x3pin Header, Rm2.54 Harwin M20-8760342	LDDC Programming Header
P5	DVI Molex 74320-1004	DVI
P6	6pin PicoBlade, Rm1.25 Molex 53398-0671	SMBus
P7	2pin PicoBlade, Rm1.25 Molex 53398-0271	Speaker
P8	SATA Plug, Rm1.27 Molex 67800-5002	SATA
P9	1x2pin Micro-Fit Header, Rm3.0 Molex 43650-0226	SATA
P10	Battery Holder Renata NL 5077-LF	Battery
P11	2x6pin PC/104 non stack through, press fit	ISA Bus
P12	2x6pin PC/104 non stack through, press fit	ISA Bus
PA/PB	2x32pin PC/104 non stack through, press fit	ISA Bus
PC/PD	2x20pin PC/104 non stack through, press fit	ISA Bus
PA/PB/PC/ PD	DIN41612 Style C, Rm2.54 Elco 21 8458 128 031 025	ISA Bus
P13	6pin MiniDIN Kycon KMDGX-6S-BS	PS/2
P14	DSUB9, DIN41652 Harting 09 66 162 681 2	COM1
P15	2x2pin Datamate, Rm2.0 Harwin M80-82 8 04 45 P	USB Port 4
P16	2x2pin Datamate, Rm2.0 Harwin M80-82 8 04 45 P	USB Port 5
P17	RJ45 with int. Magnetics, Gigabit Tyco 2-1840408-6	ETH1
P18	RJ45 with int. Magnetics, Gigabit Tyco 2-1840408-6	ETH2
P19	RJ45 with int. Magnetics, Gigabit Tyco 2-1840408-6	ETH3
P20	Double USB Type A Kycon KUSBX-A2N-B	USB0/1

Connector /Header ID	Type	Comment
P21	Double USB Type A Kycon KUSBX-A2N-B	USB2/3
P23	2x5pin Header, Rm2.54 FCI 20021521-00010D4LF	HDA
P24	6pin PicoBlade, Rm1.25 Molex 53398-0671	Backlight
P26	2x6pin Dubox, Rm2.54 FCI 89898-306ALF	SATA
P27	CompactFlash Type I, 50pin 3M N7G24-A0B2-RB-10-OHT	CFast
P28	7pin PicoBlade, Rm1.25 Molex 53398-0771	PIC Programming Header
P29	2pin Header, Rm2.54 JST B 2B-XH-A	Battery Header
P30	DSUB9, DIN41652 Harting 09 66 162 681 2	CAN1
P31	DSUB9, DIN41652 Harting 09 66 162 681 2	CAN2
P32	18pin Picoflex Molex 90816-0318	RGMII
P33	6pin PicoBlade, Rm1.25 Molex 53398-0671	SPI

Tab. 2 List of connectors

Connector/ Header ID	Type	Comment
J1	2x2pin Header, Rm2.54 Samtec TSM-102-01-L-DV-P-TR	BIOS INIT# BIOS DISABLE#
J2	2x2pin Header, Rm2.54 Samtec TSM-102-01-L-DV-P-TR	Watchdog Timeout
J3	1x8pin Header, Rm2.54 Harwin M20-8770842	LPC
J4	1x6pin Header, Rm2.54 Harwin M20-8770642	JTAG
J6	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	PS/2
J7	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	COM2
J8	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	COM3
J9	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	COM4
J10	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	COM5
J11	2x5pin Header, Rm2.54 Samtec TSM-105-01-L-DV-P-TR	COM6
J13	4pin PicoBlade, Rm1.25 Molex 53398-0471	Power Supply
J16	2x2pin Header, Rm2.54 Samtec TSM-102-01-L-DV-P-TR	Shield/GND Connection
J18	2x3pin Header, Rm2.54 Harwin M20-8760342	DDC Programming Header
J19	1x3pin Header Samtec TSM-103-01-L-SH-P-TR	Battery Activation Bottom side
J21	2x2pin Header, Rm2.54 Samtec TSM-102-01-L-DV-P-TR	CAN1
J22	2x2pin Header, Rm2.54 Samtec TSM-102-01-L-DV-P-TR	CAN2

Tab. 3 List of headers

Connector/Header ID	Type	Comment
S4	Switch Bourns 7914S	Reset Button
S5	2pin DIL Switch Copal CHS-02B	COM4 (RS485)
S9	Rotary coded Switch, 16 positions Copal S-7050ETA	Rotary Hex Switch
S12	2pin DIL Switch Copal CHS-02B	External On/Off Power Fail
S14	Rotary coded Switch, 16 positions Copal S-7050ETA	Power Management Mode
S15	2pin DIL Switch Copal CHS-02B	PWM Mode
S16	2pin DIL Switch Copal CHS-02B	LVDS Configuration
S17	2pin DIL Switch Copal CHS-02B	CAN1/COM5 Configuration
S18	2pin DIL Switch Copal CHS-02B	CAN2/COM6 Configuration
S19	2pin DIL Switch Copal CHS-02B	COM5 Half/Full Duplex
S20	2pin DIL Switch Copal CHS-02B	COM6 Half/Full Duplex

Tab. 4 List of switches

3.2. Memory and I/O resources

3.2.1. General memory layout and configuration

The IPC/BL71 uses the same memory layout as a standard desktop PC. Onboard devices, DRAM, graphics controller and Boot Block Flash make use of the 4 GByte addressable memory space. Tab. 5 shows a typical configuration of the IPC/BL71

Address			Size	Device / Register	Remarks
0000'0000h	-	0009'FFFFh	640K	Main Memory (DRAM)	
000A'0000h	-	000B'FFFFh	128K	Embedded Media and Graphics Driver Function 0	
000C'0000h	-	000D'FFFFh	128K	System Board	
000E'0000h	-	000E'FFFFh	64K	System Board	
000F'0000h	-	000F'FFFFh	64K	System Board	
7F70'0000h	-	7F7F'FFFFh	1M	System Board	
7F80'0000h	-	7FFF'FFFFh	8M	System Board	
8000'0000h	-	FFFF'FFFFh	2G	PCI Bus	

Tab. 5 Physical Memory Address Space Layout for IPC/ML71

Important note

The main memory above 1M isn't fully usable for applications. The main memory for applications is shared with the graphics memory (UMA: Unified Memory Architecture).
BIOS and other System devices use memory above 1MB. Depending on enabled or disabled functions in the BIOS the amount of additional memory used can vary.

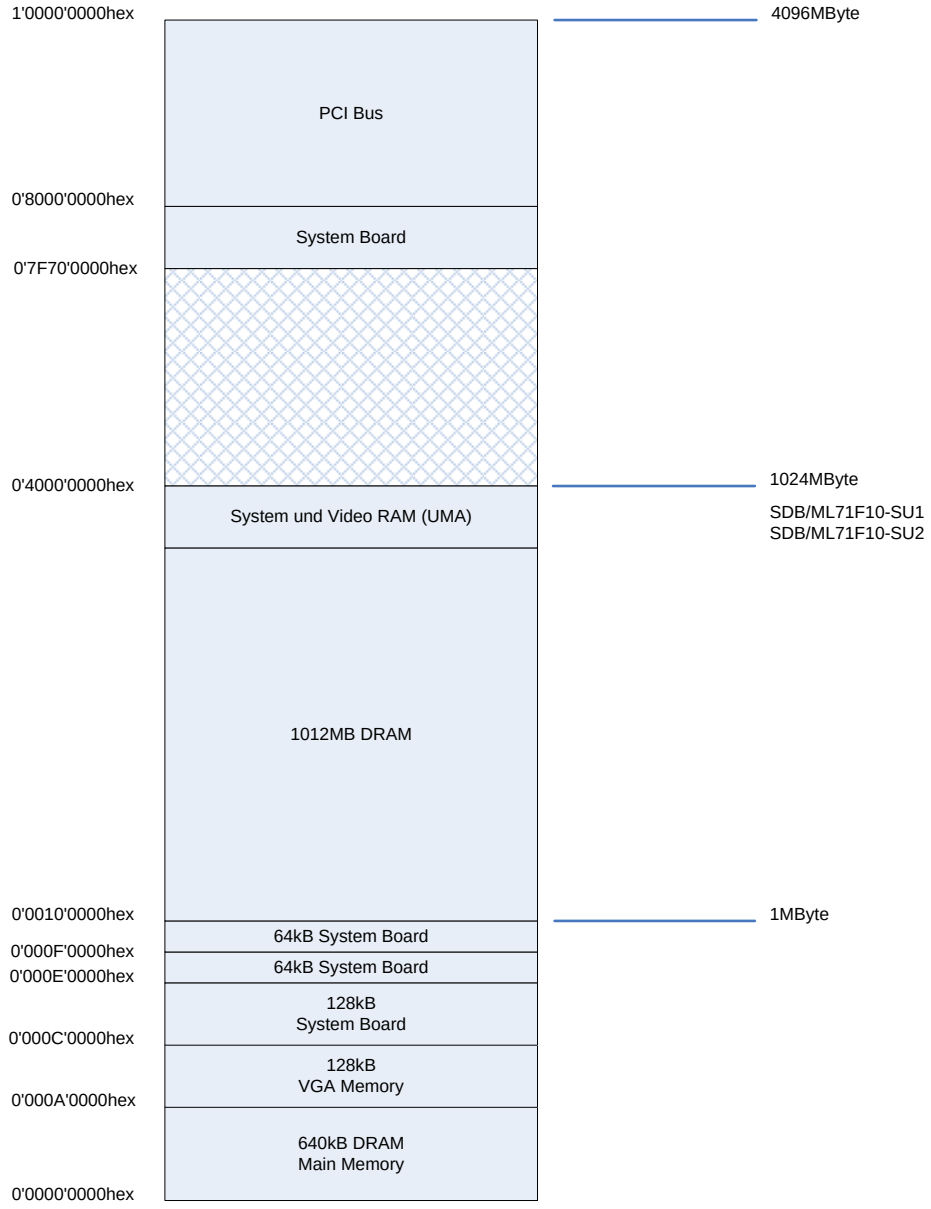


Fig. 3 Memory map

3.2.2. General I/O Layout and configuration

The IPC/BL71's 64 kbyte I/O address space is mapped to the PC/104 bus address space as indicated in the table below. Note that 16 bit address decoding should be used on all PC/104 expansion boards to make efficient use of the I/O address space.

Address			Size	Device / Register	Remarks
0000h	-	000Fh	16 Bytes	Slave DMA (8237)	
0020h	-	0021h	2 Bytes	PIC master (8259)	command/status
0040h	-	0043h	4 Bytes	PIT (8254)	
0060h	-		1 Byte	Keyboard/mouse	data port
0061h	-		1 Byte	Port B	control
0064h			1 Byte	keyboard/mouse	command/status
0070h	-	0071h	2 Bytes	RTC RAM	address/data port

0072h	-	0073h	2 Bytes	high RTC RAM	address/data port
0080h			1 Byte	POST code	
0081h	-	0083h	2 Bytes	DMA (8237)	
0087h			1 Byte	DMA (8237)	
0089h	-	008Bh	3 Bytes	DMA (8237)	
008F			1 Byte	DMA (8237)	
0092h			1 Byte	Port A	
00A0h	-	00BFh	32 Bytes	PIC slave (8259)	Command/Status
00C0h	-	00DF	32 Bytes	DMA (8237)	
00F0h			1 Byte	Numeric Data Processor	
00C4					
0200h	-	022F	48 Bytes	Free	avail. On PC/104 bus
0278	-	027Fh	16 Bytes	reserved for LPT2	
02A8h	-	02Afh	8 Bytes	COM6	
02E0	-	02Efh	16 Bytes	free	avail. On PC/104 bus
02F8	-	02FFh	8 Bytes	COM2	
0300h	-	036Fh		free	avail. On PC/104 bus
0370h	-	0372h	3 Bytes	reserved for Floppy 2	Legacy, not available
0374h	-	0375h	2 Bytes	reserved for Floppy 2	Legacy, not available
0377h			1 Bytes	reserved for Floppy 2	Legacy, not available
0378h	-	037Fh	8 Bytes	reserved for LPT2	Legacy, not available
03A8h	-	03Afh	8 Bytes	COM5	
03B0h	-	03BBh	11 Bytes	VGA adapter	
03BCh	-	03BFh	4 Bytes	reserved for LPT3	Legacy, not available
03C0h	-	03CFh	8 Bytes	VGA adapter	EGA
03D0h	-	03DFh	8 Bytes	VGA adapter	CGA
03E0h	-	03EFh	16 Bytes	free	avail. On PC/104 bus
03F0h	-	03F2h	3 Bytes	reserved for Floppy 1	Legacy, not available
03F4h	-	03F5h	2 Bytes	reserved for Floppy 1	Legacy, not available
03F6h			1 Byte	primary IDE channel	Legacy, not available
03F7h			1 Byte	reserved for Floppy 1	Legacy, not available
03F8h	-	03FFh	8 Bytes	COM1	
0481h	-	0483h	2 Bytes	DMA high page	
0487h			1 Bytes	DMA high page	
0489h	-	048Bh	3 Bytes	DMA high page	
048Fh			1 Byte	DMA high page	
04D0h	-	04D1h	2 Bytes	PIC	Level/Edge
0500h	-	07FFh	2048 Bytes	runtime registers SIO	Refer to Datasheet
0A78h			1 Byte	PnP	Configuration port
0CF8h	-	0CFFh	8 Bytes	PCI	Configuration register
2000h	-	2FFF	4096 Bytes	PCI-PCI bridge	
3000h	-	3FFFh	4096 Bytes	PCI-PCI bridge	
4000h	-	401Eh	29 Bytes	USB controller	
4020h	-	403Eh	29 Bytes	USB controller	
4040h	-	405EH	29 Bytes	USB controller	
4060h	-	406Eh	15 Bytes	IDE controller	

4070h	-	4076h	7 Bytes	VGA controller	
7600h	-	76FFh	256 Bytes	Free	avail. On PC/104 bus
7600h	-	76FFh	256 Bytes	CAN1	
7700h	-	77FFh	256 Bytes	Free	avail. On PC/104 bus
7700h	-	77FFh	256 Bytes	CAN2	
7800h	-	7FFFh	2048 Bytes	Free	avail. On PC/104 bus
8000h	-	80FFh	256 Bytes	Free	avail. On PC/104 bus
8100h	-	81FFh	256 Bytes	Free	avail. On PC/104 bus
8200h	-	821Fh	16 Bytes	IPC/BL71 system registers	
8220h	-	82DFh	192 Bytes	free	avail. on PC/104 bus
8300h	-	83FFh	256 Bytes	Free	avail. On PC/104 bus
8400h	-	84FFh	256 Bytes	Free	avail. On PC/104 bus
8500h	-	85FFh	256 Bytes	Free	avail. On PC/104 bus
8600h	-	8600h	256 Bytes	Free	avail. On PC/104 bus
8700h	-	87FFh	256 Bytes	Free	avail. On PC/104 bus
8800h	-	88FFh	256 Bytes	Free	avail. On PC/104 bus
8900h	-	8900h	256 Bytes	Free	avail. On PC/104 bus
8A00h	-	8AFFh	256 Bytes	Free	avail. On PC/104 bus
8B00h	-	8BFFh	256 Bytes	Free	avail. On PC/104 bus
8C00h	-	8CFFh	256 Bytes	Free	avail. On PC/104 bus
8D00h	-	8DFFh	256 Bytes	Free	avail. On PC/104 bus
8E00h	-	8EFFh	256 Bytes	Free	avail. On PC/104 bus
8F00h	-	8FFFh	256 Bytes	Free	avail. On PC/104 bus
0'D000h	-	0'EFFFh	1024 Bytes	Reserved for PCI device	VGA, LAN, USB, IDE

Tab. 6 I/O address space layout

Only the I/O addresses which are marked with "avail. On PC/104 bus" can be accessed on the aforementioned connector and be used for additional peripherals. The other unused I/O space can't be accessed because these cycles are claimed by the integrated South Bridge and not by the PCI/ISA Bridge.

3.3. Intel Atom E6xxT Processor

The Intel Atom E6xx Processor Family (Codename Tunnelcreek) is a highly integrated x86 processor for embedded applications.

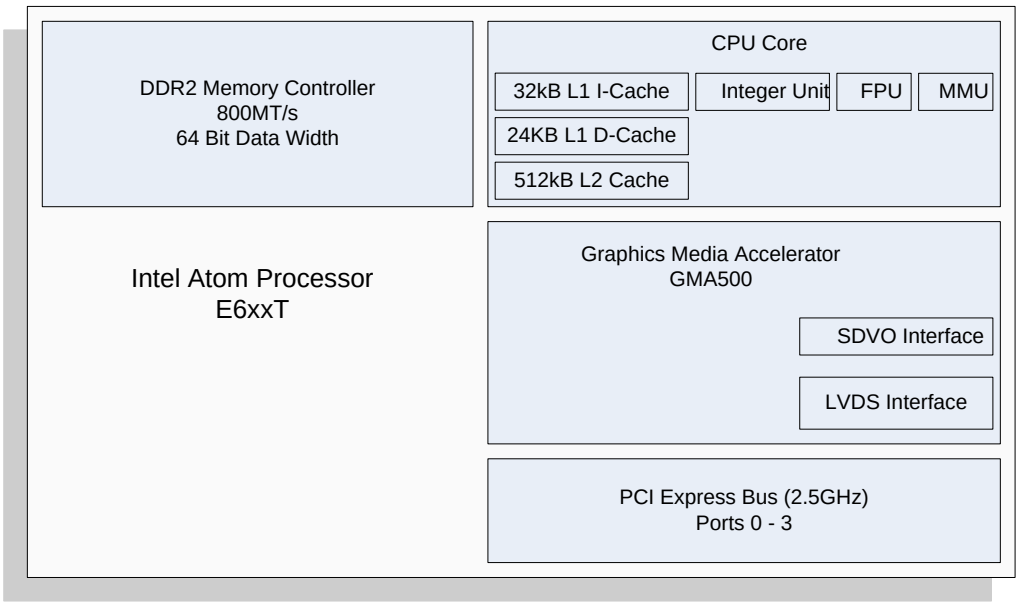


Fig. 4 Intel Atom Processor E6xx

3.4. PCI/PCIe devices

All devices follow the PCI 2.2 and PCIe 1.0a specification. The BIOS (and/or OS) controls memory and I/O resources.

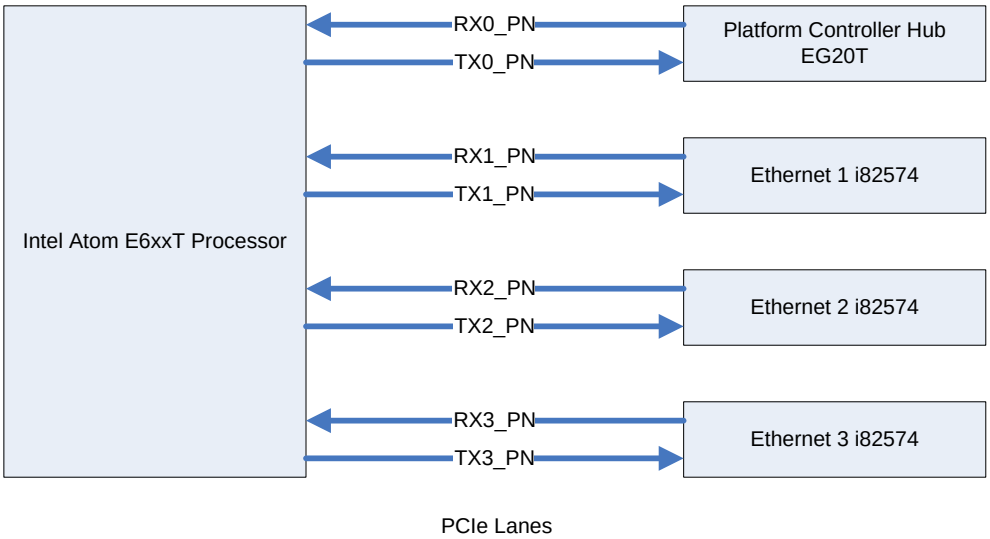


Fig. 5 PCI Express Subsystem

3.5. Intel Platform Controller Hub EG20T

The Intel Platform Controller Hub EG20T companion device (Codename Top Cliff) is designed to work with the Atom E6xx processor. The Platform Controller Hub is connected to the CPU using a PCIe lane.

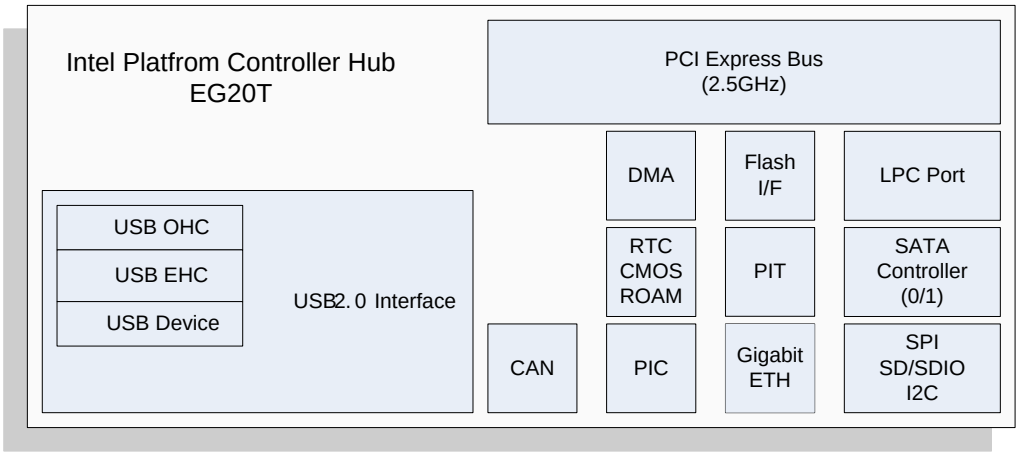


Fig. 6 Intel Platform Controller Hub EG20T

PCI Device	Vendor ID	Device ID	Bus/ Device/ Function	Interrupt Pin INTline	Comment
Intel Host Controller	8086	4114h	00/00/00		
Intel Host Controller	8086	8183h	00/01/00		
Intel VGA Controller	8086	4108h	00/02/00	A/16	
Intel Video Device	8086	8182h	00/03/00	A/11	
PCI-to-PCI Bridge	8086	8184h	00/17/00	A/16	PCIe
PCI-to-PCI Bridge	8086	8185h	00/18/00	A/17	PCIe
PCI-to-PCI Bridge	8086	8180h	00/19/00	A/18	PCIe
PCI-to-PCI Bridge	8086	8181h	00/1A/00	A/19	PCIe
ISA Bridge	8086	8186h	00/1F/00	-/-	
PCI-to-PCI Bridge	8086	8800h	01/00/00	A/16	
Intel Controller	8086	8801h	02/00/00	-/-	Packet Hub
GbE	8086	8802h	02/00/01	A/16	
Controller	8086	8803h	02/00/02	A/16	GPIO
USB Host #1 (OHCI0)	8086	8804h	02/02/00	B/19	
USB Host #1 (OHCI1)	8086	8805h	02/02/01	B/19	
USB Host #1 (OHCI2)	8086	8806h	02/02/02	B/19	
USB Host #1 (EHCI)	8086	8807h	02/02/03	B/19	
USB Device	8086	8808h	02/02/04	B/19	
System Device	8086	8809h	02/04/00	C/7	SDIO #0
System Device	8086	880Ah	02/04/01	C/7	SDIO #1
AHCI Controller	8086	880Bh	02/06/00	D/17	SATA II
USB Host #0 (OHCI0)	8086	880Ch	02/08/00	A/16	
USB Host #0 (OHCI1)	8086	880Dh	02/08/01	A/16	
USB Host #0 (OHCI2)	8086	880Eh	02/08/02	A/16	

PCI Device	Vendor ID	Device ID	Bus/ Device/ Function	Interrupt Pin INTline	Comment
USB Host #0 (EHCI)	8086	880Fh	02/08/03	A/16	
Intel Controller	8086	8810h	02/10/00	B/19	DMA
Serial Device	8086	8811h	02/10/01	B/11	UART #0
Serial Device	8086	8812h	02/10/02	B/11	UART #1
Serial Device	8086	8813h	02/10/03	B/11	UART #2
Serial Device	8086	8814h	02/10/04	B/11	UART #3
Intel Controller	8086	8815h	02/12/00	C/7	DMA
Intel Controller	8086	8816h	02/12/01	C/7	SPI
Intel Controller	8086	8817h	02/12/02	C/18	I2C
CANbus Controller	8086	8818h	02/12/03	C/18	CAN
Intel Controller	8086	8819h	02/12/04	C/18	IEEE1588 block

Tab. 7 PCI devices EG20T

The interrupt resources are assigned automatically by the BIOS and can be modified through a special setup screen (see chapter 3.6).

3.6. Hardware interrupts

The Intel Atom processor E6xx chipset integrates two legacy 8259-compatible Programmable Interrupt Controllers (PIC). The registers of the PIC can be accessed through the I/O ports 020h and 021h resp. 0A0h and 0A1h.

Device	IRQ	PCI IRQ	Comment
8254 Timer	0	-	Legacy
Keyboard	1	-	Legacy
8259	2	-	Slave controller
UART	3	-	COM2
UART	4	-	COM1
COM3	5	-	COM3
COM4	6	-	COM4
COM5	7	-	COM5 (if disabled no IRQ)
COM6	7	-	COM6 (if disabled no IRQ)
PCI	7		Reserved for PCI devices
RTC	8	-	Legacy
ACPI	9	-	Reserved
PCI	10	-	Reserved for PCI devices
PCI	11	-	Reserved for PCI devices
Mouse	12	-	Legacy
FPU	13	-	Legacy
IDE	14	-	Reserved for PCI devices
CAN	15	-	CAN1 and CAN2

Tab. 8 Hardware interrupt table

The interrupt and PnP resource are automatically allocated by the BIOS. In the setup screen "*PnP/PCI Configurations*" each interrupt can be reserved for a special peripheral device. During startup the PCI bus enumeration won't assign a reserved interrupt to a PnP/PCI device.

3.7. DMA channels

DMA	Data Width	System Resource
0	8 bits	Available
1	8 bits	Available
2	8 bits	Available
3	8 bits	Available
4		Reserved, cascaded with channel
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

Tab. 9 DMA channels

3.8. Peripheral devices

3.8.1. Scope

The peripheral devices described in this chapter are the core features of the IPC/BL71 board. Meaning that they're available on all derivates. Special features implemented only on one special board are described in a separate chapter of this documentation.

3.8.2. DVI interface

The DVI (Digital Visual Interface) signals are available on the High Density DVI-D connector P5 for direct connection of DVI compatible monitors. The signals from the SDVO (Serial Digital Video Out) port are converter into DVI signals from the controller uses the standard VGA register interface. All configurations are done by software (BIOS, VGA-BIOS).

Device connection

Pin Number	Signal	Remarks
1	DATA#2	
2	DATA2	
3	Shield 2/4	Connected to GND
4	DATA#4	Not connected
5	DATA4	Not connected
6	DDC_CLK	
7	DDC_DATA	
8	NC	Not connected
9	DATA#1	
10	DATA1	
11	Shield 1/3	Connected to GND
12	DATA#3	Not connected
13	DATA3	Not connected
14	VCC5	+5Vdc
15	GND	
16	HPDET	Hot Plug Detect
17	DATA#0	

18	DATA0	
19	Shield 0/5	Connected to GND
20	DATA#5	
21	DATA5	
22	Shield CLK	Connected to GND
23	CLK	
24	CLK#	
C1	VGA_RED	Not connected
C2	VGA_GREEN	Not connected
C3	VGA_BLUE	Not connected
C4	HSYNC	Not connected
C5	VGA_GND	Not connected

Tab. 10 DVI-D connector P5

Pin Number	Signal	Remarks
1	SD_PROM	
2	nc	not connected
3	GND	Ground
4	SC_PROM	
5	+V3.3S	3.3V supply
6	+V5S	5V supply

Tab. 11 DDC programming header J18

Important note
Do not connect J18, factory use only.

3.8.3. LVDS

The IPC71 supports a Low Voltage Differential Signaling (LVDS) interface with a pixel color depth of 18 and 24 bits. The maximum resolution is 1280x768 @ 60Hz. The pixel clock is specified between 19.75MHz up to 80MHz.

Device connection

Pin Number	Signal	Remarks
1	+V3.3S	VCC_LVDS (3.3V)
2	+V3.3S	VCC_LVDS (3.3V)
3	GND	Ground
4	GND	Ground
5	LVDS_N0	
6	LVDS_P0	
7	GND	Ground
8	LVDS_N1	

Pin Number	Signal	Remarks
9	LVDS_P1	
10	GND	Ground
11	LVDS_N2	
12	LVDS_P2	
13	GND	Ground
14	LVDS_CLK_N	
15	LVDS_CLK_P	
16	GND	Ground
17	LVDS_N3	
18	LVDS_P3	
19	MODE	
20	HMODE	

Tab. 12 LVDS connector P3

Important note

Do not draw more than 1.0A from VCC_LVDS (max. 0.5A per pin). This interface is intended for case internal use only and is not fused.

Pin Number	Signal	Remarks
1	+V12	12V supply
2	+V12	12V supply
3	GND	Ground
4	GND	Ground
5	BUFDISPEN	Display Enalbe
6	BRIGHT	Brightness

Tab. 13 Backlight connector P24

Pin Number	Signal	Remarks
1	LDDC_DAT	
2	n/c	
3	GND	
4	LDDC_CLK	
5	+V3.3S	3.3V supply
6	+V5S	5V supply

Tab. 14 LDDC programming header P4

Important note

Do not connect P4, factory use only.

The brightness of the backlight can be controlled through the 8 bit PWM register placed at I/O address 820Dhex (chapter 4.2.3). The value FFhex equals maximum brightness.

Configuration Options

Switch	Configuration	Remarks
S15:1	open = Brightness/PWM signal range 0..5V closed = Brightness/PWM signal range 0..3.3V	
S15:2	open = Analog voltage closed = PWM signal	

Tab. 15 Brightness configuration

Switch	Configuration	Remarks
S16:1	open = n/a closed = n/a	Check display manufacturer
S16:2	open = n/a closed = n/a	Check display manufacturer

Tab. 16 LVDS configuration

3.8.4. SATA/CFast-interface

Two SATA ports are available. The support SATA 1.5Gps Generation 1 an d3Gbps Generation 2 speeds and are compliant with the Serial ATA Specification 2.6 and AHCI Revision 1.1.
External SATA devices are connected through the standard SATA data connector P8. A CompactFlash card may be directly plugged in the on board CompactFlash connector P8.

Device connection

Pin Number	Signal	Remarks
S1	SGND	
S2	RxP	
S3	RxN	
S4	SGND	
S5	TxN	
S6	TxP	
S7	SGND	
PC1	CDI	Not connected
PC2	GND	Not connected
PC3	NC	Not connected
PC4	NC	Not connected
PC5	NC	Not connected
PC6	NC	Not connected
PC7	GND	Not connected
PC8	LED1	Not connected
PC9	LED2	Not connected
PC10	IO1	Not connected
PC11	IO2	Not connected
PC12	IO3	Not connected
PC13	PWR	Not connected
PC14	PWR	Not connected
PC15	GND	
PC16	GND	
PC17	CDO	Not connected

Tab. 17 CFast Connector P27(SATA Channel 0)

Pin Number	Signal	Remarks
1	GND	
2	TX+	
3	TX-	
4	GND	
5	RX-	
6	RX+	
7	GND	
8	G1	
9	G2	

Tab. 18 SATA Data Connector P8 (SATA Channel 1)

Pin Number	Signal	Remarks
1	VCC	+5V
2	GND	

Tab. 19 SATA Power Connector P9

Alternatively the SATA channel 1 signals are also available on P26. An additional converter board can be mounted onto P26 which allows either to use a second CFast or even CompactFlash device. Please contact the manufacturer for further details.

Pin Number	Signal	Remarks
1	GND	
2	GND	
3	RX-	
4	RX+	
5	GND	
6	GND	
7	TX-	
8	TX+	
9	GND	
10	GND	
11	+V5S	+5V
12	+V5S	+5V

Tab. 20 SATA Connector P26 (SATA Channel 1)

3.8.5. Serial port 1 (RS232)

The serial port COM1 has a fixed base address of 3F8H. It uses hardware interrupt 4. The resources for can be modified in the BIOS setup.

Device connection

The Serial Port COM1 is available on the DSUB9 connector P14

Pin Number	Signal	Remarks
1	DCD#	
2	RXD	
3	TXD	
4	DTR#	
5	GND	
6	DSR#	
7	RTS#	
8	CTS#	
9	RI#	

Tab. 21 Serial Port COM1 on DSUB9 P14

3.8.6. Serial port 2 (RS232)

The serial port COM2 has a fixed base address of 2F8H. It uses hardware interrupt 3. The resources for can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	DCD#	
2	DSR#	
3	RXD	
4	RTS#	
5	TXD	
6	CTS#	
7	DTR#	
8	RI#	
9	GND	
10	VCC	+5V

Tab. 22 Serial port COM2 on J7

COM2 can also be made available on the front of the enclosure through a flatwire cable. The pinout of the standard DSUB9 connector is as follows:

Pin Number	Signal	Remarks
1	DCD#	
2	RXD	
3	TXD	
4	DTR#	
5	GND	
6	DSR#	
7	RTS#	
8	CTS#	
9	RI#	

Tab. 23 Serial Port COM2

3.8.7. Serial port 3 (RS232)

COM3 is available on an internal header. The resources for COM3 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	DCD#	
2	DSR#	
3	RXD	
4	RTS#	
5	TXD	
6	CTS#	
7	DTR#	
8	RI#	
9	GND	
10	VCC	+5V

Tab. 24 Serial port COM3 on J8

3.8.8. Serial port 4 (RS232)

COM4 is available on an internal header. The resources for COM3 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	DCD#	
2	DSR#	
3	RXD	
4	RTS#	
5	TXD	
6	CTS#	
7	DTR#	
8	RI#	
9	GND	
10	VCC	+5V

Tab. 25 Serial port COM4 on J9

3.8.9. Serial port 4 (RS485)

On some baseboards serial port 4 is implemented as a non-isolated, half-duplex RS485 interface. COM4 is available on an internal header. The resources and RS485 specific modes (auto directions) for COM4 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	n/c	
2	n/c	
3	n/c	
4	n/c	
5	DATA-	
6	DATA+	
7	n/c	
8	n/c	
9	GND	
10	VCC	+5V

Tab. 26 Serial port COM4 (RS485) on J9

Configuration Options

Switch	Configuration	Remarks
S5:1	open = no termination closed = 120Ωtermination	
S5:2	n/a	do not use

Tab. 27 RS485 configuration options

3.8.10. Serial port 5 (RS232)

COM5 is only a 4 pin interface and is available on an internal header. The resources for COM5 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	NC	
2	NC	
3	RXD	
4	RTS#	
5	TXD	
6	CTS#	
7	NC	
8	NC	
9	GND	
10	VCC	+5V

Tab. 28 Serial port COM5 on J10

3.8.11. Serial port 5 (RS485)

On some baseboards serial port 5 is implemented as an isolated half-/full-duplex RS485 interface. COM5 is available on P30. The resources and RS485 specific modes (auto directions) for COM5 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	n/c	not connected
2	(DATA-)	
3	DATA-	
4	n/c	not connected
5	GND	isolated GND
6	n/c	not connected
7	(DATA+)	
8	DATA+	
9	n/c	not connected

Tab. 29 Serial port COM5 (half duplex, RS485) on P30

Pin Number	Signal	Remarks
1	n/c	not connected
2	RX-	
3	TX-	
4	n/c	not connected
5	GND	isolated GND
6	n/c	not connected
7	RX+	
8	TX+	
9	n/c	not connected

Tab. 30 Serial port COM5 (full duplex, RS485) on P30

Configuration options

Switch	Configuration	Remarks
S17:1	open = no termination closed = 120Ωtermination	
S17:2	open = full-duplex closed = half-duplex	must match S19
Switch	**Configuration**	**Remarks**
S19:1	open = full-duplex closed = half-duplex	must match S17:2
S19:2	open = full-duplex closed = half-duplex	

Tab. 31 RS485 configuration options

3.8.12. Serial port 6 (RS232)

COM6 is only a 4 pin interface and is available on an internal header. The resources for COM6 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	NC	
2	NC	
3	RXD	
4	RTS#	
5	TXD	
6	CTS#	
7	NC	
8	NC	
9	GND	
10	VCC	+5V

Tab. 32 Serial port COM6 on J11

3.8.13. Serial port 6 (RS485)

On some baseboard serial port 6 is implemented as an isolated half-/full-duplex RS485 interface. COM6 is available on P31. The resources and RS485 specific modes (auto directions) for COM6 can be modified in the BIOS setup.

Device connection

Pin Number	Signal	Remarks
1	n/c	not connected
2	(DATA-)	
3	DATA-	
4	n/c	not connected
5	GND	isolated GND
6	n/c	not connected
7	(DATA+)	
8	DATA+	
9	n/c	not connected

Tab. 33 Serial port COM 6(half duplex, RS485) on P31

Pin Number	Signal	Remarks
1	n/c	not connected
2	RX-	
3	TX-	
4	n/c	not connected
5	GND	isolated GND
6	n/c	not connected
7	RX+	
8	TX+	
9	n/c	not connected

Tab. 34 Serial port COM6 (full duplex, RS485) on P31

Configuration options

Switch	Configuration	Remarks
S18:1	open = no termination closed = 120Ωtermination	
S18:2	open = full-duplex closed = half-duplex	must match S20
Switch	**Configuration**	**Remarks**
S20:1	open = full-duplex closed = half-duplex	must match S18:2
S20:2	open = full-duplex closed = half-duplex	

Tab. 35 RS485 configuration options

3.8.14. USB interface

The IPC/ML71xxx-xxxE features an OHCI/EHCI compatible USB Hostcontroller having assigned the base address and IRQ at boot time by the PCI-BIOS. Four channels are available. USB2 can be configured as a USB device.

Device connection

The USB interface uses two dual USB connectors.

P20 (top) Pin Number	USB channel 0 Signal	P20 (bottom) Pin Number	USB channel 1 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 36 USB ports 0 and 1 on P20

P21 (top) Pin Number	USB channel 2 Signal	P21 (bottom) Pin Number	USB channel 3 Signal
1	VBUS	1	VBUS
2	D-	2	D-
3	D+	3	D+
4	GND	4	GND

Tab. 37 USB ports 2 and 3 on P21

USB Ports 4 and 5 are available on internal connectors P15 and P16

P15 Pin Number	USB channel 4 Signal	P16 Pin Number	USB channel 5 Signal
1	D+	1	D+
2	D-	2	D-
3	VBUS	3	VBUS
4	GND	4	GND

Tab. 38 USB ports 4 and 5 on P15 and P16

Important note

The USB power supplies on P20, P21, P15 and P16 are not protected against short circuit.

Important note

Maximum cable length allowed for keyboard and mouse connection is 3 m.
Use shielded cables for maximum EMI protection.

3.8.15. USB Device

Device connection

The USB Device uses a standard USB mini-B connector.

Pin Number	Signal	Remarks
1	VBUS	
2	D-	
3	D+	
4	Not connected	
5	GND	

Tab. 39 USB device P22 (on bottom side of the PCB)

Important note

The USB power supply on P22 is not protected against short circuit.

3.8.16. Ethernet interfaces

The IPC/ML71xxx-xxxE features two or three PCIe Gigabit-Ethernet controller having assigned the base address and IRQ at boot time by the BIOS. On some systems a third Gigabit-Ethernet controller is available.

There are two LED's (yellow and green) integrated into the RJ45 connector. The green LED indicates speed. The LED will be on at 1000Mbps and off at 10/100Mbps. The yellow "activity" LED indicates either link or activity. When a link is established the LED is on, if not the LED is off. Activity means sending or receiving data and is indicated by the yellow LED blinking.

No configuration options are available for the ethernet device.

Device connection

The Ethernet interface uses the standard RJ45 connector P17, P18 and P19 for 100Ω shielded or unshielded Twisted Pair cabling.

Pin Number	Signal	Remarks
1	TX+	
2	TX-	
3	RX+	
4-5	line termination	
6	RX-	
7-8	line termination	

Tab. 40 Ethernet twisted pair interface connector P17, P18 and P19 (RJ45)

3.8.17. RGMII

Reduced Gigabit Media Independent Interface is routed from the CPU directly to P32 (Molex Picoflex 18pin, 90816-0318)

Device connection

Pin Number	Signal	Remarks
1	RGMII_RD0	
2	RGMII_TD0	
3	RGMII_RD1	
4	RGMII_TD1	
5	RGMII_RD2	
6	RGMII_TD2	
7	RGMII_RD3	
8	RGMII_TD4	
9	RGMII_RXC	
10	RGMII_TXC	
11	RGMII_RXCTL	
12	RGMII_TXCTL	
13	RGMII_MDC	
14	RGMII_MDIO	
15	RGMII_RST#	
16	+V3.3S	3.3V supply
17	GND	Ground
18	+V3.3S	3.3V supply

Tab. 41 RGMII P32

The power supplies aren't protected.

3.8.18. System Management Bus (I2C)

The SMBus host controller integrated in the E6xx allows the processor to communicate with SMBus Slaves. The interface is compatible with most I2C devices. The interface complies with the System Management Bus (SMBus) Specification 1.0.

Device Name	7 Bit Address	Description
DA6011	0x69	ATOM E6xx power chip
BIOS EEPROM	0x57	EEPROM for saving BIOS settings
DB400	0x6E	PCIe clock repeater controller

Tab. 42 SMBus connected slaves

Device connection

Pin Number	Signal	Remarks
1	SMB_CLK	Clock
2	SMB_DAT	Data
3	SMB_ALRT#	Alert
4	+V5S	5V supply
5	+V3.3S	3.3 supply
6	GND	Ground

Tab. 43 SMB/I2C P6

The power supplies aren't protected.

3.8.19. Serial Peripheral Interface

An external SPI memory device is available to store persistent data.

Device connection

Pin Number	Signal	Remarks
1	MOSI	
2	MISO	
3	CS#	Chip Select
4	CLK	Clock
5	+V3.3S	3.3V supply *
6	GND	

Tab. 44 SPI P33

The power supply is not protected.

3.8.20. High Definition Audio

INTEL High Definition Audio interface is integrated in the ATOM E6xx processor.

Device connection

Pin Number	Signal	Remarks
1	SDATA_IN	
2	SDATA_OUT	
3	RST#	Reset
4	SYNC	
5	GND	
6	BITCLK	
7	GND	
8	SPKR	
9	+V5S	5V supply *
10	+V3.3S	3.3V supply *

Tab. 45 HDA P23

The power supplies are not protected!

Pin Number	Signal	Remarks
1	BUZ+	5V supply
2	BUZ-	

Tab. 46 Speaker P7

3.8.21. PS/2 Keyboard/Mouse interface

The keyboard signals are only available on an internal header J6. However a MiniDIN (PS/2 connector) can be mounted optionally instead of P21 (USB channels 2 and 3). The controller uses hardware interrupt 1 for the keyboard and hardware interrupt 12 for the mouse. The following configuration options are provided:

Device connection

The standard PS/2 connector P13 is not mounted by default. The PS/2 signals are available on the internal header J6 (2x5 pin). P13 is used (if available) for direct connection of the keyboard or mouse (depending on jumper configuration).

Pin Number	Signal	Pin Number	Signal
1	KBDATA	2	KBCLK
3	P3-1	4	P3-5
5	MDATA	6	MCLK
7	P3-2	8	P3-6
9	GND	10	+5V (not fused)

Tab. 47 Keyboard/Mouse internal header J6 (2x5 pin)

Configuration options

Jumper	Configuration	Remarks
J6	Pin 1-3, 2-4 closed = Keyboard signals on P13 Pin 3-5, 4-6 closed = Mouse signals on P13 Pin 1-3, 2-4, 3-5, 4-6 closed = all signals on P13	Only if P13 is mounted

Tab. 48 Keyboard/Mouse configuration options

3.8.22. JTAG

Important note
Do not connect factory use only.

Device connection

Pin Number	Signal	Remarks
1	TCK	
2	TDO	
3	TMS	
4	TDI	
5	+V3.3A	3.3V supply
6	Ground	Ground

Tab. 49 JTAG interface header J4

3.8.23. LPC

Do not connect.

Device connection

Pin Number	Signal	Remarks
1	LAD0	Adress/Data
2	LAD1	
3	LAD2	
4	LAD3	
5	FRAME#	Frame
6	RST#	Reset
7	CLK	Clock
8	SERIRQ	Serial interrupt

Tab. 50 LPC interface header J3

3.8.24. Rotary Switch

A Hex-Switch (S9) is assembled on the board. The value can be read through an I/O command at the address 820C hex (please refer to chapter 4.2.3 for further details).

3.8.25. Watchdog

The watchdog timer is configurable for 100 ms or 1.6 s timeout. Once timed out, it may activate the IPC/BL71's hardware reset.

Configuration Options

Jumper	Configuration	Remarks
J2	Pin 1-3 open = 1.6 s Pin 1-3 closed = 100 ms	

Tab. 51 Watchdog configuration options

Important note

Make sure that the application is able to trigger the watchdog every 50ms to 80ms when enabling a 100ms watchdog timeout.

3.8.26. PC/104 Bus Interface

The PC/104 bus interface of the IPC/BL71 allows expansion with a wide range of I/O and communications boards. The bus interface is described in the IEEE 996 and 996.1 standards documentation. The bus connector pinout is shown below.For single board applications only the power pins should be connected. See paragraph 7.1 for electrical specification.

Pin		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*	*Pin*		*Signal Name*
						A1	⊗	IOCHCK#	B1	⊗	GND
P11			P12			A2	⊗	SD7	B2	⊗	RESETDRV
1	⊗	GND	1	⊗	GND	A3	⊗	SD6	B3	⊗	+5V
2	⊗	SMB_DAT	2	⊗	+5V	A4	⊗	SD5	B4	⊗	IRQ9
3	⊗	SMB_CLK	3	⊗	SMB_ALRT#	A5	⊗	SD4	B5	⊗	-5V (not used)
4	⊗	Vbatt	4	⊗	STOP*	A6	⊗	SD3	B6	⊗	DRQ2
5	⊗	+V12	5	⊗	+V12	A7	⊗	SD2	B7	⊗	-12V (not used)
6	⊗	GND	6	⊗	GND	A8	⊗	SD1	B8	⊗	0WS#
D0	⊗	GND	C0	⊗	GND	A9	⊗	SD0	B9	⊗	+12V (not used)
D1	⊗	MEMCS16#	C1	⊗	SBHE#	A10	⊗	IOCHRDY	B10	⊗	(KEY)
D2	⊗	IOCS16#	C2	⊗	LA23	A11	⊗	AEN	B11	⊗	SMEMW#
D3	⊗	IRQ10	C3	⊗	LA22	A12	⊗	SA19	B12	⊗	SMEMR#
D4	⊗	IRQ11	C4	⊗	LA21	A13	⊗	SA18	B13	⊗	IOW#
D5	⊗	IRQ12	C5	⊗	LA20	A14	⊗	SA17	B14	⊗	IOR#
D6	⊗	IRQ15	C6	⊗	LA19	A15	⊗	SA16	B15	⊗	DACK3#
D7	⊗	IRQ14	C7	⊗	LA18	A16	⊗	SA15	B16	⊗	DRQ3
D8	⊗	DACK0#	C8	⊗	LA17	A17	⊗	SA14	B17	⊗	DACK1#
D9	⊗	DRQ0	C9	⊗	MEMR#	A18	⊗	SA13	B18	⊗	DRQ1
D10	⊗	DACK5#	C10	⊗	MEMW#	A19	⊗	SA12	B19	⊗	REFRESH#
D11	⊗	DRQ5	C11	⊗	SD8	A20	⊗	SA11	B20	⊗	SYSCLK
D12	⊗	DACK6#	C12	⊗	SD9	A21	⊗	SA10	B21	⊗	IRQ7
D13	⊗	DRQ6	C13	⊗	SD10	A22	⊗	SA9	B22	⊗	IRQ6
D14	⊗	DACK7#	C14	⊗	SD11	A23	⊗	SA8	B23	⊗	IRQ5
D15	⊗	DRQ7	C15	⊗	SD12	A24	⊗	SA7	B24	⊗	IRQ4
D16	⊗	+5V	C16	⊗	SD13	A25	⊗	SA6	B25	⊗	IRQ3
D17	⊗	MASTER#	C17	⊗	SD14	A26	⊗	SA5	B26	⊗	DACK2#
D18	⊗	GND	C18	⊗	SD15	A27	⊗	SA4	B27	⊗	TC
D19	⊗	GND	C19	⊗	(KEY)	A28	⊗	SA3	B28	⊗	BALE
						A29	⊗	SA2	B29	⊗	+5V
						A30	⊗	SA1	B30	⊗	OSC
						A31	⊗	SA0	B31	⊗	GND
						A32	⊗	GND	B32	⊗	GND

Tab. 52 PC/104 bus connectors PA/PB, PC/PD

Important note

For proper operation ***all*** +5V and GND pins must be connected with short, low impedance lines to the main power supply.

Important note

Do not connect bus drivers/receivers with integrated bushold circuit to the PC/104 signals. This may disturb proper operation of the IPC/BL71 board or add-on boards.

The battery backup supply for the onboard RTC (Real Time Clock) is connected to P11 as followed and can be used for additional PC/104 boards. Note that due to the additional load the battery lifetime is decreased.

Pin Number	Signal	Remarks
1	GND	
2	SMB_DAT	
3	SMB_CLK	
4	Vbatt	
5	+V12	
6	GND	

Tab. 53 External Battery Connector P11 (1x6 pin)

The user programmable output signals STOP* and TRIGGER* are available on connector P12. The signal levels are TTL compatible with maximum 4 mA sink and 2 mA source output current:

Pin Number	Signal	Remarks
1	GND	
2	+5V	max. 10 mA
3	SMB_ALRT#	
4	STOP#	
5	+V12	
6	GND	

Tab. 54 User Programmable Output Connector P12 (1x6 pin)

The STOP* signal may be controlled by software (see chapter 4.2.3).

3.8.27. Power supply

The processor and its peripherals are powered by a non-isolated, integrated power supply which generates all the necessary voltages.

Pin Number	Signal	Remarks
1	+24VDC_AUX	Additional, permanent power supply
2	Power Fail/Remote on/off	Power Fail Input
3	+24VDC	+10V..+30V
4	GND	GND (/shield)

Tab. 55 Power supply connector P1 (1x4 pin)

For normal operation the external power supply has to be connected to the pins 3 (+24VDC) and 4 (GND) of the connector P1.
Pin 1 (+24VDC_AUX) may be used as a standby supply for the GoldCap RTC backup (optionally)
Pin 2 is used as an input for either a power fail or remote on/off signal.

The input voltage is also available on J13. Note that the input voltage on J13 isn't protected or filtered.

Pin Number	Signal	Remarks
1	+24VDC	+10V..+30V
2	+24VDC	same as pin 1
3	GND	GND (/shield)
4	GND	same as pin 3

Tab. 56 Power supply header J13 (1x4 pin)

Switch	Configuration	External wiring	Remarks
S12:1-2	on/off = automatic on/off mode off/on = remote on/off mode	current sinking current sourcing	check chapter 3.8.30

Tab. 57 Power supply configuration

If automatic on/off mode is configured, there is an internal pull up resistor that will automatically start the device. If it is required to toggle the Power Fail Input an external pull down (current sinking) wiring is required
Automatic on/off mode is configured by default.

If remote on/off mode is configured there is no internal pull up resistor and the input has to be supplied with an input voltage > 10V to enable the device. If it is required to toggle the Power Fail Input disconnect the external source.

Using either configuration the state of Power Fail Input can be determined reading the #PF bit in the status register (refer to chapter 4.2.3.)

In some applications it can be useful when the digital ground plane (GND) is connected to shield. In order to short circuit the two power planes two jumpers have to be placed on J16.

Jumper	Configuration	Remarks
J16	Pin 1-2 closed = shield and GND connected Pin 3-4 closed = shield and GND connected	check chapter 3.8.30

Tab. 58 Power plane short circuit

3.8.28. Backup-Battery

The processor and its peripherals are powered by a non-isolated, integrated power supply which generates all the necessary voltages.

Pin Number	Signal	Remarks
1	+VBATT	
2	GND	GND (/shield)

Tab. 59 Backup-Battery on header P29 (1x2 pin)

3.8.29. Isolated power supply

Instead of the synchronous buck controller a DC/DC converter can be soldered onto the board for isolating the power supply. The input range will be reduced. For further information please contact the manufacturer

3.8.30. Power supervision

The power management control unit (PCU) contains a RISC microcontroller and is implemented on the base board.
The PCU can be operated in two modes: power fail mode or remote on/off mode. The following two chapters describe their functionality in detail.

3.8.31. Power Fail

In power fail mode the microcontroller monitors the external power fail signal. The state of power fail signal can be accessed through the status register, I/O 8200h. In order to initiate a power fail the pin has to be pulled low. Pulling it high or leaving it floating has no effect on the flag or operation.

Application example

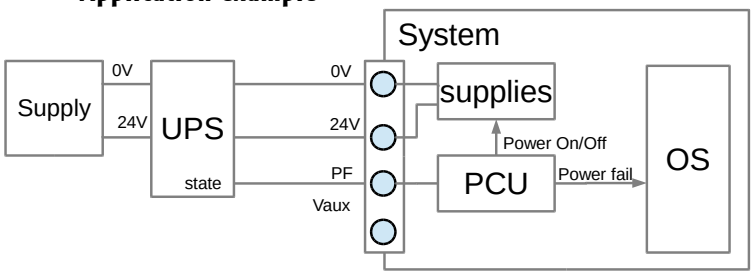


Fig. 7 Typical power fail application

The application has to poll the power fail flag and call different functions according to the state of the flag.

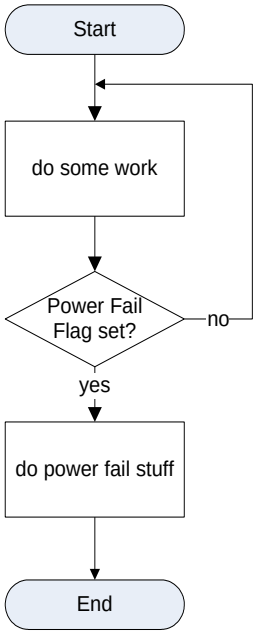


Fig. 8 Typical power fail flow

Additonally the onboard power management contol unit (PCU) can switch off the power supplies after a power fail is detected. For that the PCU has to be configured according to the parameters found in table 60.

3.8.32. Remote On/Off

With the Remote On/Off function the system can be switched on and off through an external control signal. When active the internal software goes from the run state into the shutdown state. After a predefined timeout the PCU switches the main power supply off (even if the systems hangs while closing or terminating services). The timeout can be configure through S14 (table 60). Please use the timing diagrams on the next pages for further understanding.

- Pull the remote On/Off signal to the supply voltage to start the system.
- Pull the remote On/Off signal to 0V or leave it floating to switch the system off.

Typical applications where Remote On/Off is used are mobile applications such as vehicles. To use the full functionality of the Remote On/Off feature it is required to use the pfmon software (sample code for Windows Embedded Standard OS or driver for Linux are available). The

software analyzes the state of the remote On/Off signal and triggers a proper shut down. Additionally it is possible execute user commands before shutting down such as logging off from the network, etc.

Application example

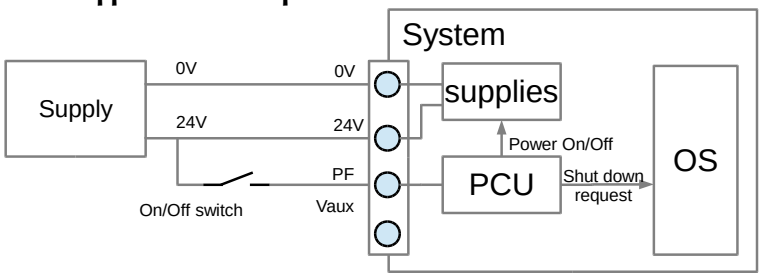


Fig. 9 Application example: Remote On/Off

Configure PCU for Power Fail or On/Off Signal

Configure the PF Signal using S12 according to table 57.
Select a timing setting using S14 according to table 60.

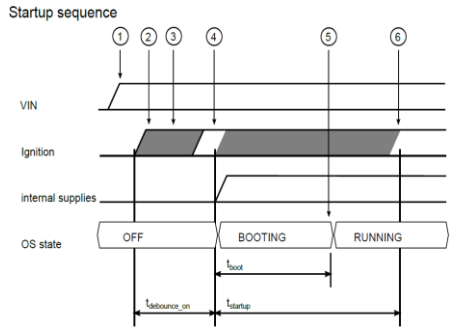
Config switch position	$t_{debounce\_on}$ On debouncing	$t_{startup}$ boot time	$t_{debounce\_off}$ Off debouncing	t_{hard_off} Hardware off delay
0	the PCU is in bypass mode (default position)			
1	2 s	15 s	60 s	1 min
2	2 s	60 s	60 s	5 min
3	2 s	30 min	60 s	2 h
4	2 s	2 h	60 s	2 h
5 – F	N/a	n/a	n/a	n/a

Tab. 60 PCU timing configuration through S14

When switch S14 is in position 0 the PCU is in bypass mode.

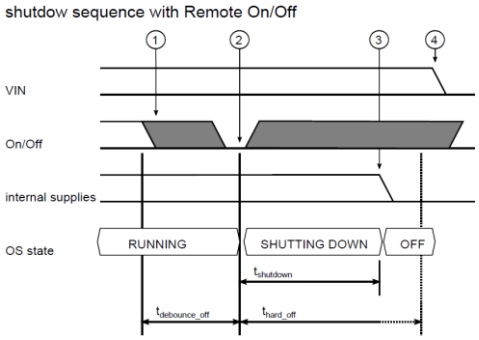
Delay time explanation

$t_{debounce\_on}$	Delay time during off mode time to prevent the system form start accidentally.
$t_{startup}$	During this time the system will not turn off again the hardware to prevent the operating system to be turned off during start up.
t_{boot}	Time while the operating system is starting. This time is independent of the PCU.
$t_{debounce\_off}$	During this time it is possible to restore the power and interrupt the PCU to turn off the hardware. Do not shut down the operating system during this period because the power is not turned off if the On/Off signal is restored.
t_{hard_off}	Starts after $t_{debounce\_off}$ has expired. After t_{hard_off} the hardware will be turned off independently if the On/Off signal has been restored.
$T_{shutdown}$	Time the operating system requires to shut down. Is independent of the PCU.



1. Power is supplied to the system.
2. On/Off signal is provided.
3. If stable for more than 2 seconds the internal supplies are enabled.
4. The system will start booting
5. Operating system has finished starting up
6. t_{statup} time has expired. Now the System is ready to be turned off again.

Fig. 10 Start-up timing diagram



1. The On/Off signal is released. If restored during $t_{debounce\_off}$ the system continues normally.
2. $t_{debounce\_off}$ has expired. The hardware is waiting for t_{hard_off} to turn off the internal supplies
3. Operating system is down.
4. Hardware is turned off

Fig. 11 Shutdown timing diagram

Important Notes

The operating system must support the remote on/off function.

3.8.33. CAN interface

There is no firmware for the CAN interface. All setup functions have to be programmed by the user or configured by a third-party device driver.

Important Note

For detailed information and configuration options of the SJA1000 Stand Alone CAN Controller please refer to the appropriate documentation 1.5.3.

I/O base address configuration

The registers of the CAN controller can only be accessed in the I/O address space. The I/O base addresses cannot be configured. CAN1 is located at I/O 7600hex and CAN2 at I/O 7700hex.

Interrupt configuration

Both channels use interrupt IRQ15.

Device connections

The IPC/ML71 has two DSUB9 connectors for each channel.

Pin	Signal Designation	Signal
1	-	not used
2	CAN_L	CAN_L
3	CAN_GND	signal ground
4	-	not used
5	-	not used
6	-	not used
7	CAN_H	CAN_
8	-	not used
9	-	not used

Tab. 61 Pin assignment of CAN interface: CAN1 at P30 / CAN2 at P31

The CAN signals can also be found on the internal headers J21 and J22. These headers are used to connect the connectivity board onto the main board. The connectivity board is used when two DSUB9 connector for each CAN interface are needed. The connectivity board provides an additional DSUB9 connector for each channel. The same pinout for the DSUB9 female connectors are used as in the table above.

J21	CAN Interface 1	J22	CAN Interface 2
Pin Number	Signal	Pin Number	Signal
1	GND	1	GND
2	CAN1_H	2	CAN2_H
3	GND	3	GND
4	CAN1_L	4	CAN2_L

Tab. 62 CAN interfaces 1 and 2 on J21 and J22

A 120Ωtermination resistor is implemented on the base board module.

S17:1	Termination CAN1
on	active
off	not active

Tab. 63 Terminatino resistor

S18:1	Termination CAN2
on	active
off	not active

Tab. 64 Termination resistor

3.9. Hardware limitations

3.9.1. Peripheral limitations

- COM5/COM6 are 4 pin interfaces

3.9.2. ISA bus limitations

- The interrupt lines are pulled up with 8k2 resistors to Vcc (EISA specification) instead of 2k2 (IEEE 996)
- NMI (IOCHCK#) is not supported on the PC/104 bus
- 16 bit cycles are not supported on the PC/104 bus
- memory cycles are not supported on the PC/104 bus
- Only a predefined amount of I/O addresses are available on the PC/104 bus, please refer to the appropriate chapter for details

4 Programming information

4.1. Overview

The programming of the IPC/BL71 board is done with standard memory and I/O read and write operations. Most configuration options are handled by the BIOS.

4.2. Interrupt, memory and I/O resources

4.2.1. Interrupt resources

Please refer to chapter 3.6 for the table showing the usage of the IPC/IPC/BL71's interrupts.

4.2.2. Memory resources

Will be inserted in a future release of this document.

4.2.3. I/O resources

This paragraph describes only the system register and support functions not directly related to a specific peripheral device. The general I/O layout is shown in paragraph 0. Peripheral devices are discussed in paragraph 0.

Address	Device / Register	Remarks
8200h	Status Register	
8201h	Control Register	
8202h	Function ID Register	
8203h	Reserved	FFhex, do not write
8204h	Option ID Register	
8205h	Setup Register	
8206h	Logic Design Revision Register	do not write
8207h	Reserved	FFhex, do not write
8208h	Reserved	FFhex, do not write
8209h	Reserved	FFhex, do not write
820Ah	Reserved	FFhex, do not write
820Bh	I2C Register	for Temp Sensor
820Ch	Button Register	Write clears status
820Dh	PWM Register	Write to clear flags
820Eh..821Eh	Reserved	FFhex, do not write
821Fh	Test Register	Factory use only

Tab. 65 IPC/ML71 and IPC/SL71 System Registers

Address	Device / Register	Remarks
82E0h	Status Register	Only if CAN is available
82E1h	Reserved	do not access
82E2h	Function ID Register	Only if CAN is available
82E3h	Reserved	do not access
82E4h	Option ID Register	Only if CAN is available
82E5h	Reserved	do not access
82E6h	Revision ID Register	Only if CAN is available
82E7..82FFh	Reserved	do not access

Tab. 66 IPC/ML71 and IPC/SL71 CAN Specific System Registers

Status Register 8200h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OVERTMP	LOBAT	0	WDG#	0	0	0	PF#	Read
Do not write								Write
D0hex								Reset

Description:

OVERTMP Temperature Sensor Status Flag

Read	Write
0 = programmed temp. limit reached 1 = temperature ok (below limit)	

LOBAT Battery Status Flag

Read	Write
0 = Battery voltage low 1 = Battery voltage ok	

WDG# Watchdog Status Flag

Read	Write
0 = Watchdog has timed out 1 = Watchdog running or disabled Reset by issuing a hardware reset (see register 8204hex)	

PF# Power Fail Status Flag

Read	Write
0 = Power fail occurred (input low) 1 = No power fail occurred (input high)	

Reserved Reserved, always write 0

Control Register 8201h

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	WDTRIG	WDNMI	STOP	0	0	0	1	Read
dnw	WDTRIG	dnw	STOP	Do not write				Write
10hex								Reset

Description:

WDTRIG Watchdog Trigger

Read	Write
Last value written	Any state change triggers the watchdog.

WDNMI Watchdog NMI Configuration

Read	Write
0 = Watchdog activates hardware reset 1 = not supported	Do not write

ERROR Error Signal State

Read	Write
0 = Inactive, red LED off 1 = Active, red LED on	0 = Inactive, red LED off 1 = Active, red LED on

Function ID Register 8202h

D7	D6	D5	D4	D3	D2	D1	D0	Access
HID[7:0]								Read
Do not write								Write
same as Read value								Reset

Description:

HID HW ID

Read	Write
51h = general NETIPC board	

Option ID Register 8204h

D7	D6	D5	D4	D3	D2	D1	D0	Access
OID[7:0] Option ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

OID Option ID

Read	**Write**
C8h = IPC/ML71xxx-xxxxE C8h = IPC/SL71xxx-xxxxE	A5h = Writing data A5h invokes a complete hardware reset (also clearing the Watchdog timeout status bit)

reserved Reserved, always write 0

Setup Register 8205h

D7	D6	D5	D4	D3	D2	D1	D0	Access
RUN	WDEN	AUX	SPI_WP#	0	USB_EN2	USB_EN1	USB_EN0	Read
RUN	WDEN	AUX	SPI_WP#	0	USB_EN2	USB_EN1	USB_EN0	Write
83hex								Reset

Description:

RUN Ready bit, green LED

Read	**Write**
0 = Inactive, green LED off 1 = Active, green LED on	0 = Deactivate green LED 1 = Activate

WDEN Watchdog enable

Read	Write
0 = Watchdog disabled 1 = Watchdog enabled (running)	0 = Disable watchdog 1 = Enable watchdog

AUX Auxilary LED (green)

Read	Write
0 = LED off 1 = LED on	0 = Deactivate green LED 1 = Activate green LED

SPI_WPn SPI Write Protection

Read	Write
0 = SPI write enabled 1 = SPI write protected	0 = Allow write cycles to SPI 1 = Protect SPI memory

USB_EN2 USB Enable Group 2

Read	Write
0 = USB Ports 4/5 are disabled 1 = USB Ports 4/5 are enabled	0 = Disable USB Ports 4/5 1 = Enable USB Ports 4/5

USB_EN1 USB Enable Group 1

Read	Write
0 = USB Ports 2/3 are disabled 1 = USB Ports 2/3 are enabled	0 = Disable USB Ports 2/3 1 = Enable USB Ports 2/3

USB_EN0 USB Enable Group 0

Read	Write
0 = USB Ports 0/1 are disabled 1 = USB Ports 0/1 are enabled	0 = Disable USB Ports 0/1 1 = Enable USB Ports 0/1

Revision ID Register 82E6h

D7	D6	D5	D4	D3	D2	D1	D0	Access
RID[7:0] Revision ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

RID Logic Design Revision ID

Read	Write
see Tab. 79	

I2C Register 820Bh

D7	D6	D5	D4	D3	D2	D1	D0	Access
SCLO	SDAO	SCL	SDA	1	1	1	1	Read
SCLO	SDAO	Reserved, always write 1						Write
XFh								Reset

Description:

SCLO Clock Port Output State

Read	**Write**
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SDAO Data Port Output Port Latch State

Read	Write
0 = Pin state = low 1 = Pin state = high	0 = Output latch state = low 1 = Output latch state = high (open collector)

SCL Clock Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

SDA Data Port Pin State

Read	Write
0 = Pin state = low 1 = Pin state = high	

reserved Reserved, always write 0

Switch Register 820Ch

D7	D6	D5	D4	D3	D2	D1	D0	Access
0	0	0	0	S9_3	S9_2	S9_1	S9_0	Read
reserved, always write 0								Write
00hex								Reset

Description:

S9_3 Switch S9, bit 3

Read	Write
Data 2^3	

S9_2 Switch S9, bit 2

Read	Write
Data 2^2	

S9_1 Switch S9, bit 1

Read	Write
Data 2^1	

S9_0 Switch S9, bit 0

Read	Write
Data 2^0	

Reserved Reserved, always write 0

PWM Register 820Dh

D7	D6	D5	D4	D3	D2	D1	D0	Access
PWM preset D[7..0]								Read
PWM preset D[7..0]								Write
FFh								Reset

Description:

D[7..0] PWM Preset Register

Read	Write
D[7..0] = Preset Value	D[7..0] = Preset Value

Test Register 821Fh

D7	D6	D5	D4	D3	D2	D1	D0	Access
T7	T6	T5	T4	T3	T2	T1	T0	Read
T7	T6	T5	T4	T3	T2	T1	T0	Write
00hex								Reset

Description:

D[7..0] Test Register

Read	**Write**
D[7..0] = Preset Value	D[7..0] = Preset Value

CAN Status Register 82E0h

D7	D6	D5	D4	D3	D2	D1	D0	Access
1	1	1	CAN2_IRQ	1	1	1	CAN1_IRQ	Read
reserved, always write 0								Write
same as Read value								Reset

Description:

CAN2_IRQ CAN Channel 2 Interrupt Request

Read	**Write**
0 = IRQ pending 1 = no IRQ pending	

CAN1_IRQ CAN Channel 1 Interrupt Request

Read	Write
0 = IRQ pending 1 = no IRQ pending	

Reserved Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

CAN Function ID Register 82E2h

D7	D6	D5	D4	D3	D2	D1	D0	Access
CFID[7:0] Function ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

CFID CAN Function ID

Read	Write
6Ah = IPC/NETSBC-7AC	

reserved Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

CAN Option Register 82E4h

D7	D6	D5	D4	D3	D2	D1	D0	Access
IO_MEM2*	0	0	1	IO_MEM1*	0	0	1	Read
reserved, always write 0								Write
same as Read value								Reset

Description:

IO_MEM2* CAN Channel 2 Adressing Mode

Read	Write
0 = I/O mode 1 = not available	

IO_MEM1* CAN Channel 1 Adressing Mode

Read	Write
0 = I/O mode 1 = not available	

Reserved Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

CAN Revision ID Register 82E6h

D7	D6	D5	D4	D3	D2	D1	D0	Access
CRID[7:0] Function ID								Read
reserved, always write 0								Write
same as Read value								Reset

Description:

RID CAN Revision ID

Read	Write
see Tab. 79	

reserved Reserved, always write 0

This register is only available on devices (and boards) where a CAN interface is implemented.

4.3. Peripheral devices

4.3.1. Serial ports

The Serial Port interfaces use the standard PC/AT register set. The Serial Port controller is compatible with the standard 16C550A UART with 16 byte receive and transmit FIFOs. For detailed programming information please refer to the IBM PC/AT Technical Reference, the Texas Instruments TL16C550C datasheet or similar documentation. I/O base addresses and IRQ can be modified through BIOS.

4.3.2. Keyboard/Mouse interface

The Keyboard/Mouse interface uses the standard PC/AT register set. The keyboard controller is compatible with the standard Intel 82C42 device with integrated keyboard host controller firmware. For detailed programming information please refer to the IBM PC/AT and PS/2 Technical Reference, the Intel 82C42PC datasheet or similar documentation.

4.3.3. Ethernet interfaces

On the IPC/IPC/BL71 board the Ethernet interfaces use the Intel 82574 Gigabit Ethernet Controller. For detailed programming information and drivers check www.syslogic.com or www.intel.com .

4.3.4. Temperature sensor

The Temperature Sensor is built up using an LM75 compatible temperature sensor programmable through an I2C interface. The I2C interface programming is done through the I2C Register of the IPC/BL71. The LM75 can be accessed at the I2C address 00h. For detailed programming information please refer to the National Semiconductor LM75 datasheet or similar documentation.
Poweron default setting for OVERTMP* is 80°C chip temperature.

I2C Address	Device	Remarks
00h	LM75	

Tab. 67 I2C Address Space

4.3.5. Watchdog

The watchdog is disabled by default on power-on and must be enabled either by the BIOS or by the application program.

If watchdog programming is done from application software level, before enabling the watchdog by setting the WDEN bit in the Setup Register.
The watchdog generates a hardware reset if it is not triggered within the configured timeout window by writing the WDTRIG bit in the Control Register. The application must check the WDG* bit in the Status Register upon startup to identify the Watchdog as the source of the reset, and it must issue a hardware reset (by writing the value 0a5h to the Option ID Register) to clear the WDG* flag. Otherwise the system resets again as soon as the Watchdog is started.
For sample code please contact Syslogic.

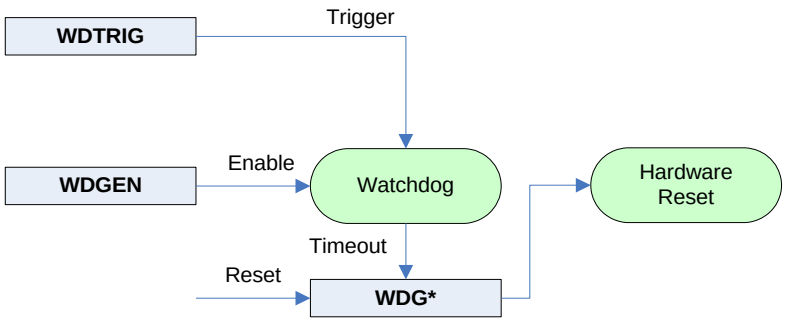


Fig. 12 Watchdog Blockdiagram

The watchdog can only initiate a hardware reset. The NMI option is not supported.

4.3.6. CAN interface

The CAN interface uses the stand-alone controller SJA1000 from NXP. For detailed programming information please refer to the datasheet and the application note mentioned in chapter 1.5.3.

5 Enclosure, assembly and mounting

5.1. IPC/ML71 dimensions

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see paragraph 1.5).

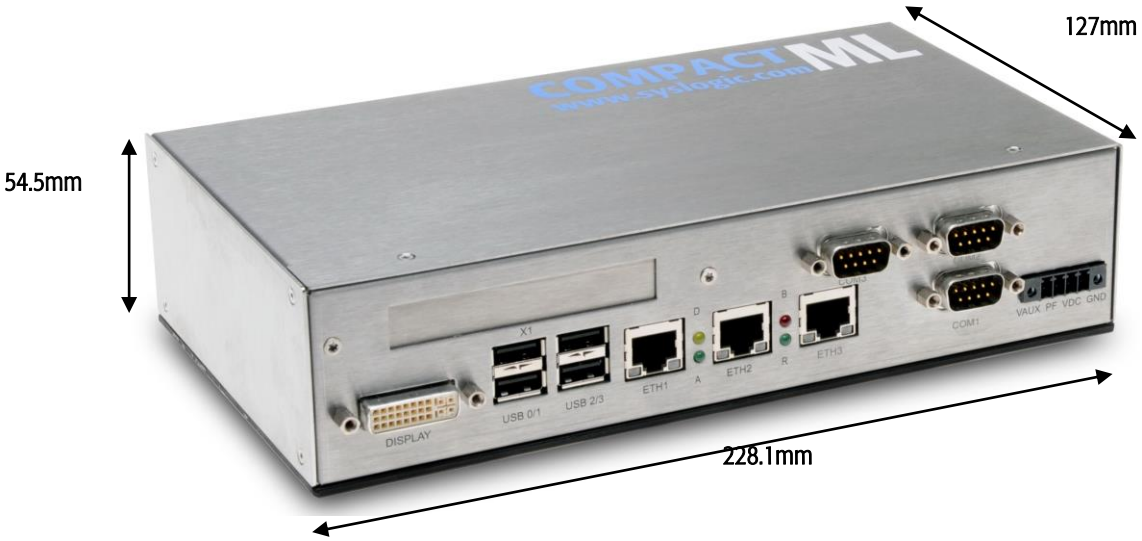


Fig. 13 IPC/ML71F16-A101E (product image may vary)

Important Notes

Before assembling the whole enclosure with the electronic modules please read through the following paragraphs containing information about the assembling of the system.

Please contact the manufacturer if you need more detailed CAD drawings of the enclosure.

5.2. Mounting options

The figure below shows the bottom view of the IPC/ML71. The marked holes show where the DIN Rail Clips are mounted.

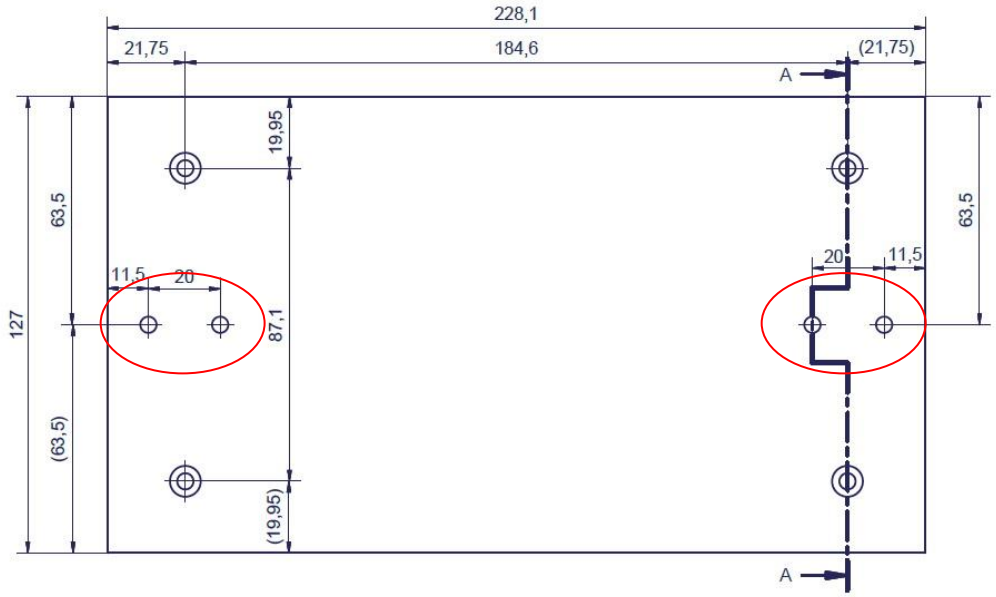


Fig. 14 Bottom view of the IPC/ML71 (product image may vary)

6 Installation and cabling

6.1. Introduction

Installation and cabling of the IPC/ML71 system has to be done with great care; the correct cabling is essential for high operational reliability and the correct grounding is necessary for protection. To meet the requirements of "CE"-certification all cables have to be shielded. The enclosure has to be connected to ground via the DIN-rail or mounting kit.

Important note

Before applying power to the IPC/ML71 system, the IPC/BL71 board must be configured correctly and mounted.

Important notes

To meet the requirements of RFI "CE"-certification, correct mounting, installation and cabling of the IPC/ML71 system according to these guidelines is absolutely necessary.

6.2. Powering the IPC/ML71 System

6.2.1. General information

The "logic voltage", i.e. the power driving the electronic circuits (CPU and base board) is applied from a 24VDC power supply (10VDC...30VDC). The internal power supply converts the input voltage to the logic voltage level. Remember that the power supply is unisolated. For an isolated version please contact the manufacturer. The input voltage is applied with a 3pin Weidmüller connector.

6.2.2. Power supply

The use of a power supply with the following requirements is mandatory:

- minimal power: 21W
- voltage range: 10…30Vdc
- efficiency > 88%
- integrated over-current limitation
- compliant with the directives 2004/1008/EC (EMC) and 2006/96/EC (LVD)
- compliant with the standards EN 61000-6-1, EN 61000-6-2, EN 61000-6-3 and EN 61000-6-4, FCC Part 15 Class B
- compliant with EN 60950-1

Syslogic recommends the use of the Syslogic DIN Rail power supply *PSU/DR24V60W* (input voltage: 230Vac, output voltage: 24Vdc, power: 60W).

Please make sure that the input voltage does not exceed 30V otherwise the base board could get damaged. If the input voltage drops below 10V the system doesn't work properly, correct operation cannot be guaranteed.

Important notes

Please read the safety and installation instructions of the power supply before connecting it to the IPC.
If connecting additional devices to the power supply the specified maximum power must not be exceeded.

6.2.3. Power connection

Pin	Description
+24VDC_AUX (1)	External power supply
Power Fail (2)	Power fail or remote on/off input
+24VDC (3)	VDC
GND (4)	Ground

Tab. 68 Power connector pinout

The connector can be ordered directly at your Weidmüller distributor (order code: *BCZ 3.81/04/180F SN SW [1792970000]*).
For normal operation only Pin 3 (+24VDC) and Pin 4 (GND) are used.

Order Code	Type
1792970000	BCZ 3.81/04/180F SN SW

Tab. 69 Weidmüller power connector

Wire cross section for connecting the power supply to the IPC device : 0.2…1.5 mm^2
Wire cross section for connecting the power supply to the AC mains : 0.5…4 mm^2

6.3. Cabling the interfaces

6.3.1. Connector locations

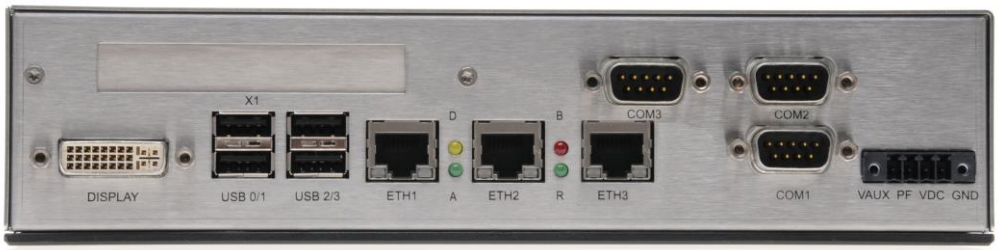


Fig. 15 Front view with connector markings (product image may vary)

Fig. 16 Side view with connector markings (product image may vary)

Fig. 17 Side view with connector markings (option with mounted connectivity board)

6.3.2. IPC/ML71F16-A101E

Connector Marking	Interface Type
DISPLAY	DVI
USB0/1	USB0 (bottom) / USB1 (top)
USB2/3	USB2 (bottom) / USB3 (top)
ETH1	Ethernet 1 (PCI device 13)
ETH2	Ethernet 2 (PCI device 12)
ETH3	Ethernet 3 (PCI device 12)
COM1	COM1: RS232
COM2	COM2: RS232 (or RS485)
COM3	COM3: RS232
COM4	COM4: RS232 (or RS485)
X1	CAN1 (I/O base 0x7600)
X2	COM6: RS485
X10	Optional Add-On Boards (
red LED	(B): Busy
green LED	(R): RUN
yellow LED	(D): Disk (SATA)
green LED	(AUX): Auxilary, user configurable
PF VDC GND	Power Supply

Tab. 70 IPC/ML71F16-A101E: Connectors

6.3.3. IPC/ML71F16-A102E

Connector Marking	Interface Type
DISPLAY	DVI
USB0/1	USB0 (bottom) / USB1 (top)
USB2/3	USB2 (bottom) / USB3 (top)
ETH1	Ethernet 1 (PCI device 13)
ETH2	Ethernet 2 (PCI device 12)
COM1	COM1: RS232
COM2	COM2: RS232 (or RS485)
COM3	COM3: RS232
COM4	COM4: RS232 (or RS485)
X1 (or CAN1)	CAN1 (I/0 base 0x7600)
X2 (or CAN1)	CAN1 (I/O base 0x7700)
red LED	(B): Busy
green LED	(R): RUN
yellow LED	(D): Disk (SATA)
green LED	(AUX): Auxilary, user configurable
PF VDC GND	Power Supply

Tab. 71 IPC/ML71F16-A102E: Connectors

6.3.1. Cable length

The maximum cable length can be taken from the table below:

Device Marking	Interface Type	Cable Length	Shielded
DISPLAY	DVI Display Interface	< 10m	Yes
ETH1	Ethernet 1	> 30m (up to 100)	Yes
ETH2	Ethernet 2	> 30m (up to 100)	Yes
ETH3	Ethernet 2	> 30m (up to 100)	Yes
USB0/1	USB0 (bottom) / USB1 (top)	< 5m	Yes
USB2/3	USB2 (bottom) / USB3 (top)	< 5m	Yes
COM1	RS232	< 15m	Yes
COM2	RS232	< 15m	Yes
COM3	RS232	< 15m	Yes
COM4	RS232	< 15m	Yes
	RS485	> 30m (up to 1200)	Yes
X1	RS232	< 15m	Yes
	RS485	> 30m (up to 1200)	Yes
	CAN	> 30m (up to 1000m @ 50kbit/s) [1]	Yes
X2	RS232	< 15m	Yes
	RS485	> 30m (up to 1200)	Yes
	CAN	> 30m (up to 1000m @ 50kbit/s) [1]	Yes
VDC/GND	Input Voltage	< 3m	No
PF	Power Fail	< 3m	No
VAUX	Auxilary Input Voltage	< 3m	No

Tab. 72 Maximum cable length of all interfaces

[1] According to CAN in Automation (CiA).

6.4. Serviceable Parts

6.4.1. General information

The IPC/ML71 contains several serviceable or replaceable parts:

- Backup-Battery
- CFast card (has to be ordered separately)
- fuse

In order to exchange the backup battery or the CFast card, you must remove the cover by executing steps 1 and 2 of the following instructions.

Important notes

When opening the enclosure you're about to handle ESD sensitive devices. Be sure that appropriate precautions have been made to your working environment. from its socket.
Ensure that the device is disconnected from the power supply.

1. Remove 4 Torx screws (M2.5x5, BN3803) on the side of the case.
2. Remove the side cover.
3. Exchange the battery or CFast card.

Fig. 18 Open side view with Reset button, battery and CFast

6.4.2. CFast

Handle the flash memory module with care. In order to simplify the removal of the memory module a small commercially available tape can be applied to the compact flash which allows an easy grab of the module.

6.4.3. Battery

Use only 3V Lithium Batteries:

- Renata CR2477N, 950mAh.
- Renata CR2450N, 540mAh.

The battery socket is coded, no wrong insertion of the backup battery should be possible. Refer to the figure above for exact orientation.

Caution! Danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.
Dispose of used batteries according to the manufacturer's instructions.

For further information please contact the manufacturer.

6.4.4. Fuse F1701

The onboard fuse prevents the destruction of the product in cause of a malfunction. The fuse must be replaced by an instructed person/technician and in an ESD protected environment. The fuse F1701 is located next to the power connector on the PCB.

1. Make sure that the device is not connected to a power supply!
2. Remove 4 Torx screws (M2.5x5, BN3803) on the top and back of the cover.
3. Remove 4 Torx screws (M2.5x5, BN3803) on the side of the case.
4. Remove 2 Torx screws (M2.5x5, BN3803) or 4 or 8 UNC4-40 DSUB screws on the side of the case.
5. Remove the cover of the case.
6. Carefully remove the fuse with a pair of tweezers or needle-nosed pliers.

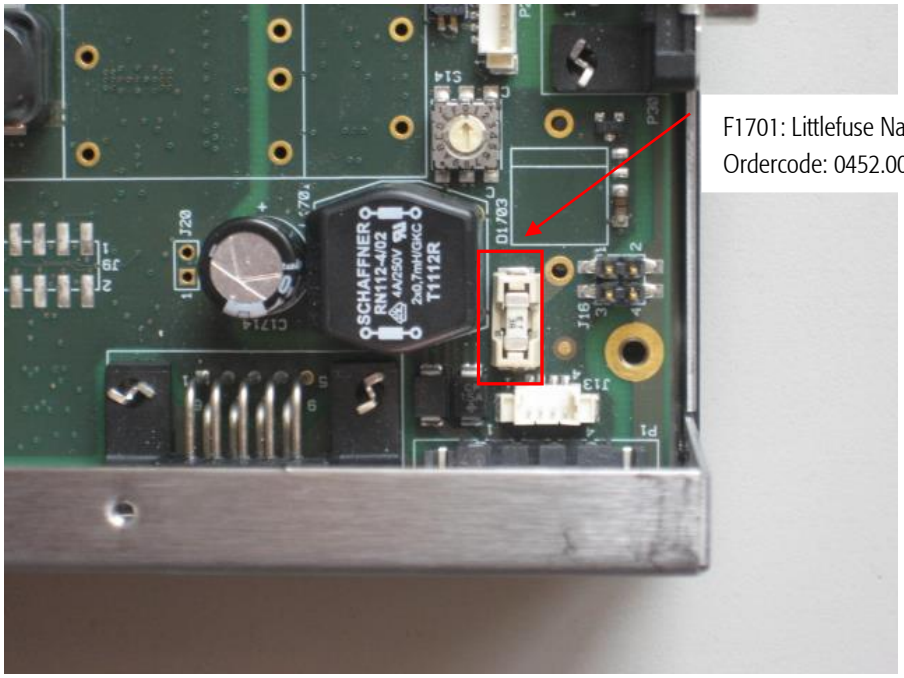


Fig. 19 Open side view with Reset button, battery and CFast

Type for F1701: Littlefuse Nano² Slo-Blo 3A: 0452.003MRL

Please note that in the code above the package code for tape and reel and quantity 1000pcs is included.

For further information on how to replace the battery please contact the manufacturer.

7 Technical data

7.1. Electrical data

Important Note

Do not operate the IPC/ML71 outside of the recommended operating conditions. Otherwise lifetime and performance will degrade. Operating the board outside of the absolute maximum ratings may damage the hardware.

Absolute maximum ratings (over free-air temperature range)

Parameter	Symbol	min	nom	max	Unit
internal power supply voltage	Vcc	-0.5		5.5	Vdc
storage temperature range [1]	Tst	-40		85	°C
Isolation CAN1 to logic [2]	V_{isol}	1000			Vrms
Isolation voltage CAN2 to logic [2]	V_{isol}	1000			Vrms
Isolation voltage CAN1 to CAN2 [2]	V_{isol}	1000			Vrms
Isolation COM5 (RS485) to logic [2]	V_{isol}	1000			Vrms
Isolation voltage COM6 (RS485) to logic [2]	V_{isol}	1000			Vrms
Isolation voltage COM5 to COM6 [2]	V_{isol}	1000			Vrms

Tab. 73 General absolute maximum ratings

[1] Due to the large effect of self-discharge at high temperature of the Lithium Battery it is recommended to store the device at around +25°C.
[2] Conditions: AC, 60s, 500m a.s.l., Ta = 25C

Recommended operating conditions

Parameter	Symbol	min	nom	max	
IPC/ML71F16-101E					
operating free-air temperature range [1]	Ta	-40		60	°C
IPC/ML71F16-102E					
operating free-air temperature range [2]	Ta	-40		63	°C
IPC/ML71F16-10xE					
operating free-air temperature range [3]	Ta	-40		65	°C
General specification					
external supply voltage	Vext	10.0	24.0	30.0	Vdc
battery backup voltage	Vbatt	2.70	3.00	3.60	Vdc
approx. battery life time @ Ta = 25°C (Tbat = 45°C) [4]	tbat		3.5		Yrs

Tab. 74 General recommended operating conditions

[1] Measured with 50% CPU load and three Gigabit Ethernet.
[2] Measured with 50% CPU load and two Gigabit Ethernet.
[3] Measured with 50% CPU load and one Gigabit Ethernet.
[4] Values calculated with a ΔT of approx. 20°C (ambient to battery) and constant ambient temperature. CR2477N battery.
Because the self-discharge of all Lithium Batteries increases rapidly at high temperatures the battery life time decreases by a great amount. For a detailed battery life time calculation the exact temperature profile has to be taken into account. Please contact the battery manufacture for further details and calculation assistance (refer to chapter 6.4.3).

The temperature range is dependent on the amount of power loss (heat) generated inside the enclosure. When for example all three Ethernet Controllers have an established link (Gigabit, S0 state) a derating has to be taken into account, approx. 3-4C for each additional Gigabit Ethernet Controller (port 2 and 3).

Electrical characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	Typ	max	Unit
IPC/ML71F16-xxxE					
External supply current @ 24Vdc, no add-ins [1]	Iext		0.54	0.61	A
Full load power dissipation @ 24Vdc, no add-ins [1]	Pmax		12.96	14.64	W
External supply current @ 10Vdc, no add-ins [2]	Iext			2.1	A
Supply current on P3 per pin	Ilvds			0.5	A
power fail: [3]					
- inactive state	PF_{high}	2.3	Vext	Vext	V
- active state	PF_{low}	-0.5	0	2.7	V
Remote on/off [2]					
- on	ENon	8.5	Vext	Vext	V
- off	ENoff	-0.5	0	7.1	V
Vbatt loading (Vcc = 5V)	Ibat(on)		22	36	uA
LOWBAT* trip voltage		2.35	2.5	2.65	V
VRT trip point (RTC Valid RAM and Time Flag)			2		V

Tab. 75 General electrical characteristics

[1] Typical value measured for IPC/ML71F16-A101E with 50% CPU load, 2 GBE ports, USB keyboard and USB mouse. Maximum value measure with 100% CPU load, 3 GBE ports, USB keyboard and USB mouse. Values for IPC/ML71F16-A102E are a bit lower.
[2] Value measured with 100% CPU load and 3 GBE ports, USB keyboard, USB mouse and 2xUSB full load.
[3] Internal pull-up resistor.

Switching characteristics
(over recommended operating range, unless otherwise noted)

Parameter	Symbol	min	nom	max	
IPC/ML71F16-xxxE					
processor clock	pclk			1.6	GHz
memory clock (DDR800)	mclk			400	MHz
memory transfer rate				800	MT/s
CAN1/CAN2 baud rate, dependant on connected nodes and bus length	canclk			1	Mbit/s
CAN clock				16	MHz
ISO high speed CAN signals			Refer to ISO 11898-24V		
General specification					
PCIe clock (1x lane)	fpcie			2.5	Gbit/s
LPC bus clock	flpc			33	MHz
ISA bus clock	fisa			8.25	MHz
COM1/COM2 baud rate				115.2	kbaud
COM3/COM4 baud rate				115.2	Kbaud
COM5/COM6 baud rate				115.2	Kbaud
ETH1/ETH2/ETH3 baud rate				1000	Mbit/s
Watchdog timeout (short period)	Tw	70	100	140	ms

Watchdog timeout (long period)	Tw	1.0	1.6	2.25	s
Timer base clock 1	fclk1		14.318		MHz
Timer base clock 1 accuracy				+/-100	ppm
Timer base clock 2	fclk2		32.768		kHz
Timer base clock 2 accuracy				+/-20	ppm
Timer base clock 2 aging				+/-3	ppm/year
Real Time Clock base clock	Fclk		32.768		kHz
Real Time Clock accuracy (25°C)				+/-20	ppm
Real Time Clock temperature coefficient				-0.04	ppm/(°C)²
Real Time Clock aging				+/-3	ppm/year

Tab. 76 General switching characteristics

7.2. EMI / EMC specification

7.2.1. Relevant standards

The IPC/ML71 with its baseboard IPC/BL71 has been designed to comply the the following standards:

- EN 55022 — Information technology equipment - Radio disturbance characteristics - Limits and methods of measurement
- EN 55024 — Information technology equipment - Immunity characteristics - Limits and methods of measurement
- EN 61000-6-2 — Electromagnetic compatibility (EMC), Part 6-2: Generic standards- Immunity for industrial environments
- EN 61000-6-4 — Electromagnetic compatibility (EMC), Part 6-4: Generic standards – Emission standard for industrial environments

7.2.2. Emission

Emission requirements according to 2004/108/EC harmonized standard EN55022 and EN61000-6-2

Test	Standard	Limit
Abstrahlung Feld	EN 61000-6-2 EN55022:2010 CISPR 22:2008	30 – 230MHz: 40dBuV/m (QP) 230 – 1000MHz: 47dBuV/m (QP) 1000 – 3000MHz: 56dBuV/m (AVG) 3000 – 6000MHz: 60dBuV/m (AVG)
Abstrahlung leitungsgebunden	EN55022:2010 CISPR 22:2008	Mains AC 0.15 – 0.5MHz: 79dBuV (QP) 0.5 – 30MHz: 73dBuV (QP) Telecommunication ports 0.15 – 0.5MHz: 97 to 87dBuV (QP) 0.5 – 30MHz: 87dBuV (QP)

Tab. 77 Emission requirements

7.2.3. Immunity

Immunity requirements according to 2004/108/EC harmonized standard EN55024 and EN61000-6-4

Test	Standard	Limit
Electro-static discharge / ESD	EN61000-4-2:2009 IEC61000-4-2:2008	6kV contact - direct 6kV contact – indirect 8kV air ➔ not applicable [1] Criterion B
RF electromagnetic field 1kHz, 80% AM	EN61000-4-3:2006 +A1:2008+A2:2010 IEC61000-4-3:2006 +A1:2007+A2:2010	80 – 1000MHz: 20V/m 1.4..2.1GHz: 10V/m 2.1..2.5GHz: 5V/m 2.5..2.7GHz: 1V/m Criterion A
Electrical fast transients / burst 5/50ns	EN61000-4-4:2004 IEC61000-4-4:2004	2.0kV Criterion B
Surge 1.2/50us	EN61000-4-5:2006 IEC61000-4-5:2005	DC power : 1kV (line - earth) 1kV (line – line) Criterion B Communication ports : 1kV (shield - earth) Criterion B
Conducted disturbances 1kHz, 80% AM	EN61000-4-6:2009 IEC61000-4-6:2008	All connections: 0.15 – 80MHz: 10V/m Criterion A

Tab. 78 Immunity requirements

[1] No air discharge applicable because no non-metallic surface is touchable

7.3. Environmental specification

The IPC/ML71 has been designed to meet the the following standards:

– EN 60068-2-27 Basic environmental testing procedures – Part 2-27:
Test Ea and guidance: Shock

– EN 60068-2-6 Environmental testing – Part 2-6:
Test Fc: Vibration (sinusoidal)

7.4. Mechanical data

The enclosure can house a complete industrial control system with many basic functions. The enclosure with its internal electronic system meets EMI/RFI electromagnetic standards according to the European "CE"- requirements (see chapter 0). If you need detailed information of the enclosure do not hesitate to contact the manufacturer. We can provide you with the technical drawings.

8 Firmware

8.1. BIOS

8.1.1. General information

The BIOS provided by Syslogic is based on the SecureCore Tiano from Phoenix Technologies. It has been customized to support onboard peripherals.

Important note

Be careful when changing the BIOS settings. The IPC system might not boot if false modifications were made. Refer to chapter 8.2 for the BIOS recovery option.

8.1.2. Main menu

In order to modify BIOS settings <F2> has to be press while booting the IPC/ML71 system.
The following main menu will appear:

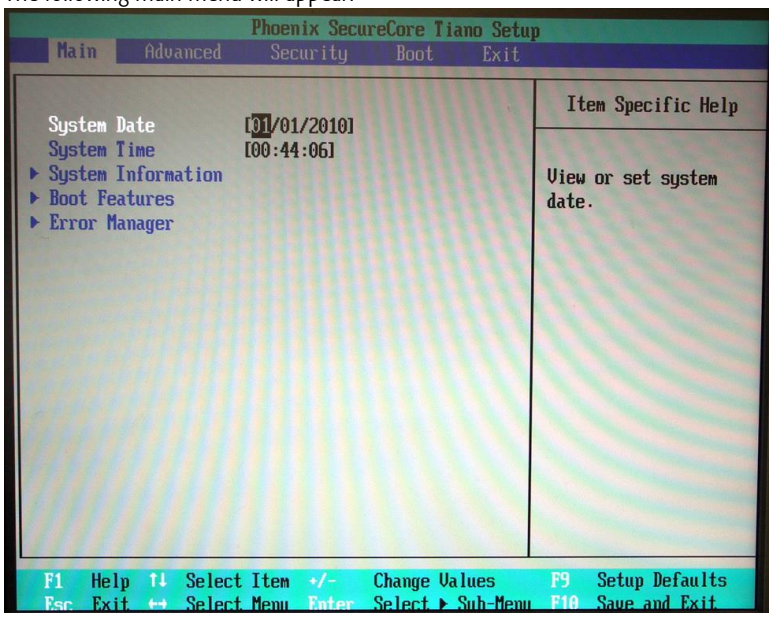


Fig. 20 BIOS setup main menu

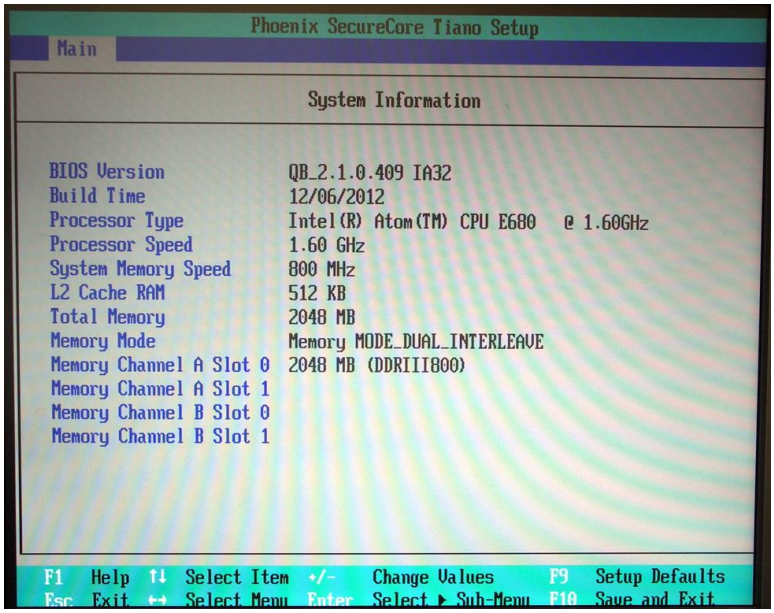


Fig. 21 System information

The system time and date can be modified in this menu. Also some system information is provided in the submenu *System Information*.

8.1.3. Advanced

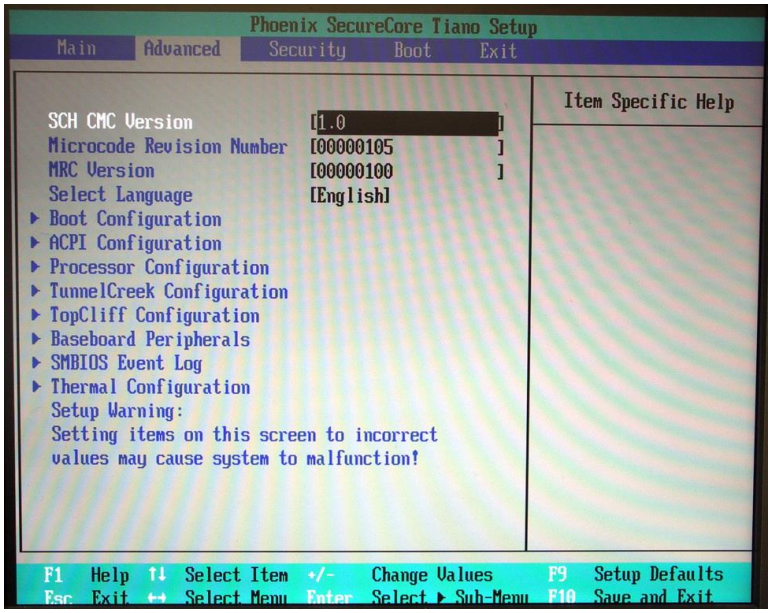


Fig. 22 Advanced menu

In the sub menu *Baseboard Peripherals* and then *SIO* different resources can be assigned to the UARTs.

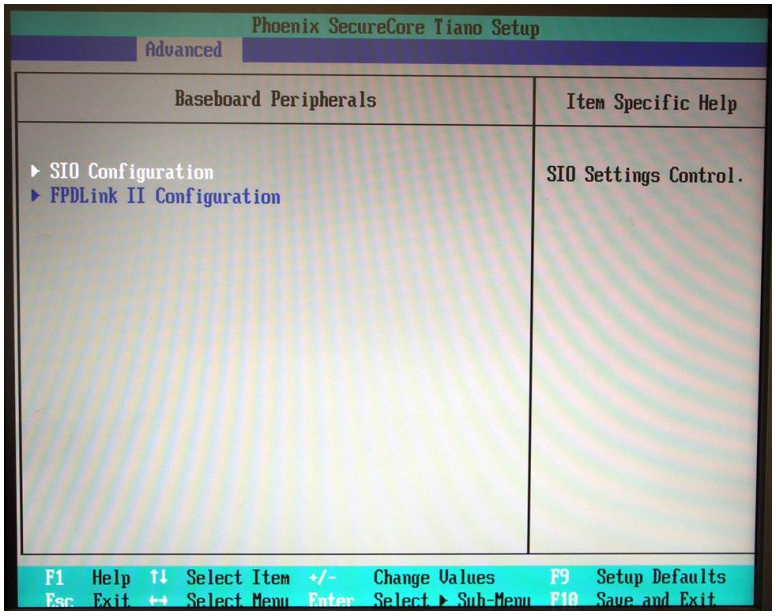


Fig. 23 Baseboard Peripherals sub menu

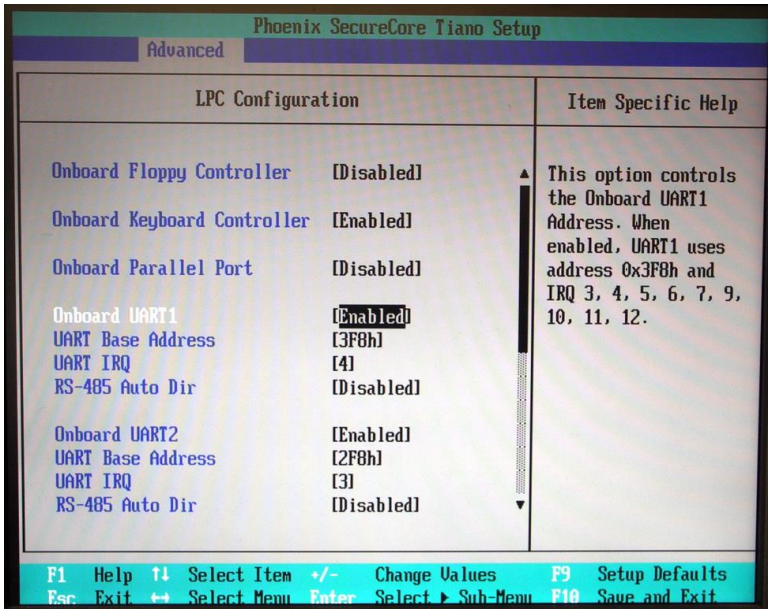


Fig. 24 SIO sub menu

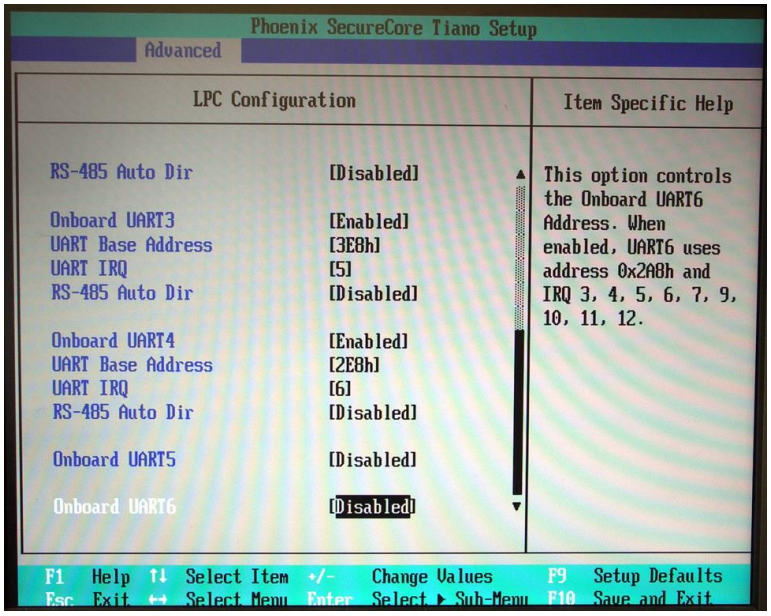


Fig. 25 UART configuration options

8.1.4. Security

No modifications should be made here.

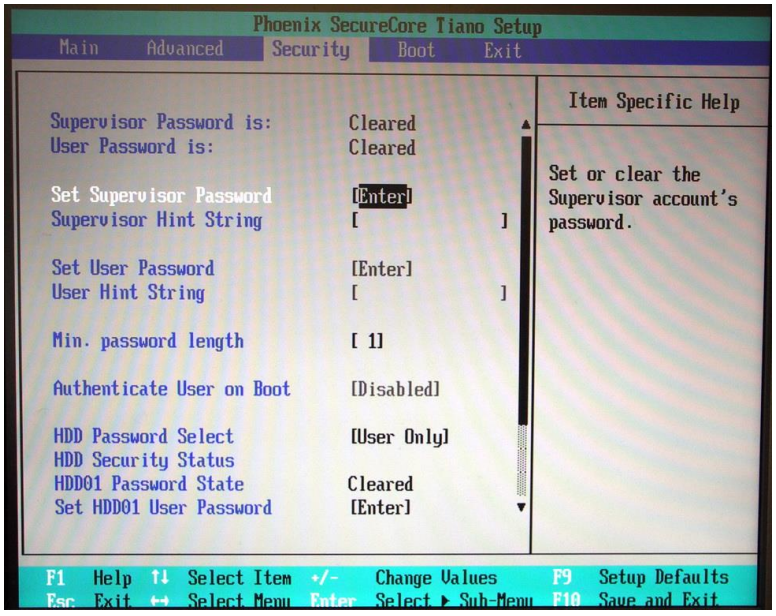


Fig. 26 Security menu

8.1.5. Boot

In this menu the boot order can be changed.

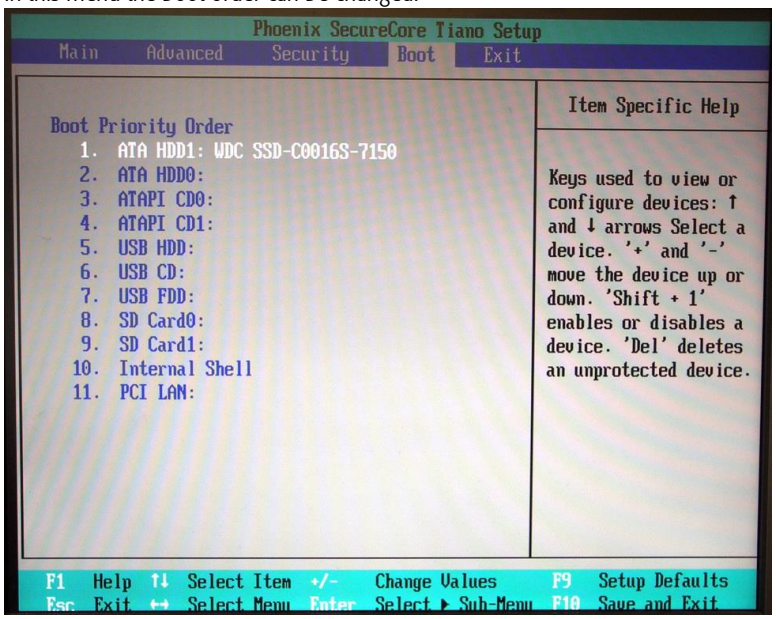


Fig. 27 Boot menu

8.1.6. Exit

Different options can be selected to exit the BIOS setup.

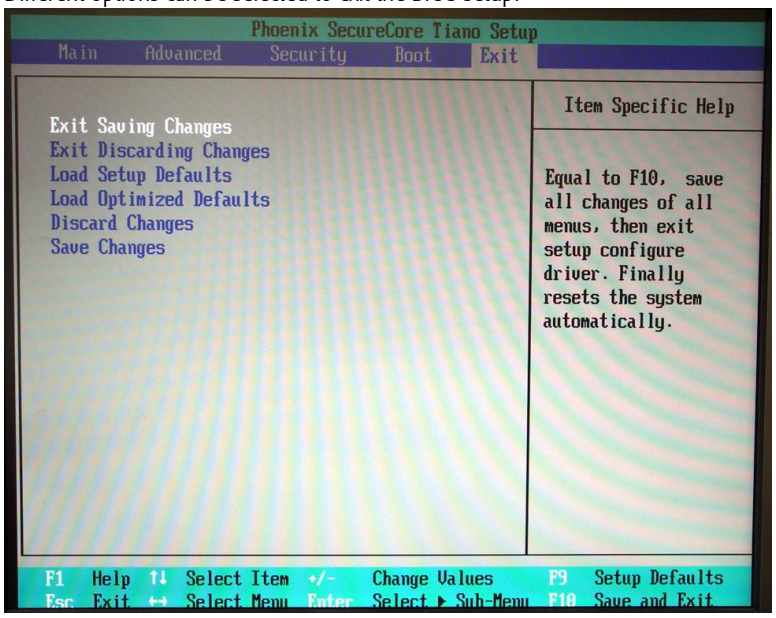


Fig. 28 Exit menu

8.2. BIOS recovery

Default BIOS settings can be loaded by short-circuiting J1 pin 1 and 2.

Important note

Ensure that the device is disconnected from the power supply. This procedure must be done by an instructed person/technician in an ESD protected environment.

1. Carefully remove the cover of the case.
2. Place a jumper onto J1:1-2.
3. Switch on the power supply.
4. Switch off the power supply after 10 seconds.
5. Remove the jumper.
6. Close the cover with the appropriate screws.

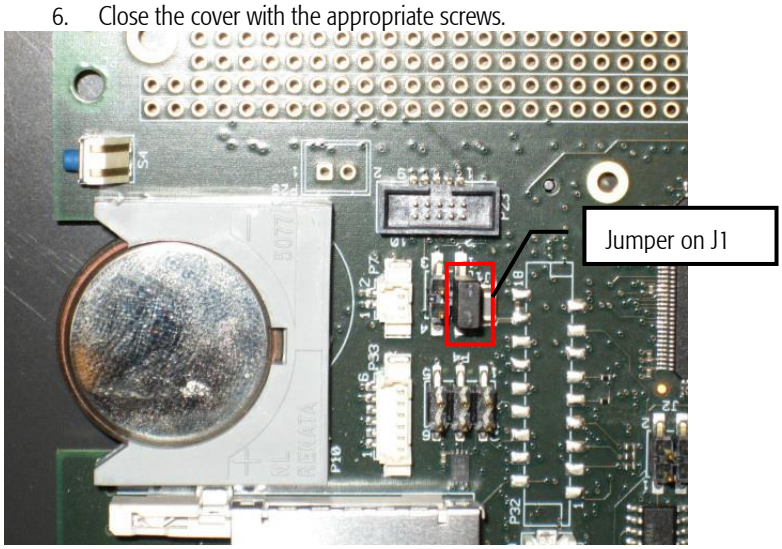


Fig. 29 Jumper on J1 :1-2 for BIOS recovery

9 Operating systems

Syslogic offers an implementation for the following operating systems (OS):

Debian Linux Distribution
IPC/DEBIAN-60A

Microsoft Windows Embedded Standard 2009
IPC/WINESTD09-71A

Microsoft Windows Embedded 7
IPC/WINESTD7-71A

Others on request.

Important note
When implementing a BSP for a new OS be sure to use the “Pentium Platform”.

10 Product revision history

10.1. Hardware

This paragraph lists the different hardware revisions of the IPC/ML71 with integrated IPC/BL71 board delivered beginning with the first production lot. Note that prototyping boards are not included and must be returned to factory for upgrade or replacement. All information listed in this document relies on definitive state hardware. Therefore this information may be incompatible with the prototyping board hardware.

Board Identification (see product label)	Product Revision	Logic Revision ID Register	Remarks
IPC/ML71F16-A101E	#1		Original Release, RoHS compliant
IPC/BL71-101E	#1	01hex	
IPC/ML71F16-A102E	#1		Original Release, RoHS compliant
IPC/BL71-102E	#1	01hex	Original Release, RoHS compliant
IPC/BL71-103E	#1	01hex	Original Release, RoHS compliant
IPC/BL71-104E	#1	01hex	Original Release, RoHS compliant
IPC/BL71-105E	#1	01hex	Original Release, RoHS compliant
IPC/ML71F16-A101E	#2		New baseboard added
IPC/BL71-101E	#2	02hex	
IPC/ML71F16-A102E	#2		New baseboard added
IPC/BL71-102E	#2	02hex	
IPC/BL71-103E	#2	02hex	
IPC/BL71-104E	#2	02hex	
IPC/BL71-105E	#2	02hex	
IPC/ML71F16-A101E	#2.1		thermal optimization
IPC/BL71-101E	#2	02hex	
IPC/ML71F16-A102E	#2.1		thermal optimization
IPC/BL71-102E	#2	02hex	
IPC/BL71-103E	#2	02hex	
IPC/BL71-104E	#2	02hex	
IPC/BL71-105E	#2	02hex	

Tab. 79 Hardware revision state

10.2. Firmware/BIOS

Board Identification (see product label)	BIOS Version	Build Date	Remakrs
IPC/ML71F16-A101E	v2a101e0	12/06/2012	Original Release
IPC/BL71-101E	v2a101e0	12/06/2012	Original Release
IPC/ML71F16-A101E	v2a102e0	12/06/2012	Original Release
IPC/BL71-102E	v2a101e0	12/06/2012	Original Release
IPC/BL71-103E	v2a103e0	12/06/2012	Original Release
IPC/BL71-104E	v2a104e0	12/06/2012	Original Release
IPC/BL71-105E	v2a105e0	12/06/2012	Original Release

Tab. 80 BIOS revision state

Important note

This document always covers the latest product revision listed in Tab. 79.
Please contact the manufacturer's technical support for upgrade options.

11 Manufacturer information

11.1. Contact

Our distributors and system integrators will gladly give you any information about our products and their use. If you want to contact the manufacturer directly, please send a fax or email message containing a short description of your application and your request to the following address or use one of the information or technical support request forms on our internet homepage:

Syslogic Datentechnik AG
Täfernstrasse 28
CH-5405 Baden-Dättwil / Switzerland

Email: info@syslogic.com
www: http://www.syslogic.com
Phone +41 (0)56 200 90 40
Fax: +41 (0)56 200 90 50

Technical support:
support@syslogic.com